ZORAN

Rev. 0.52

October, 1998

Vaddis **ZR36710**
Integrated DVD Decoder

Preliminary Data Sheet

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1. Introduction

This document provides the technical specifications of the Vaddis **ZR36710** decoder device that are needed to successfully implement this device in a system design. The material contained within is presented with the assumption that the reader is familiar with the following standards:

- MPEG-1 and MPEG-2 including video, system and audio.
- DVD, VideoCD, CD-I (FMV), CD-DA, AC-3 and S/PDIF.

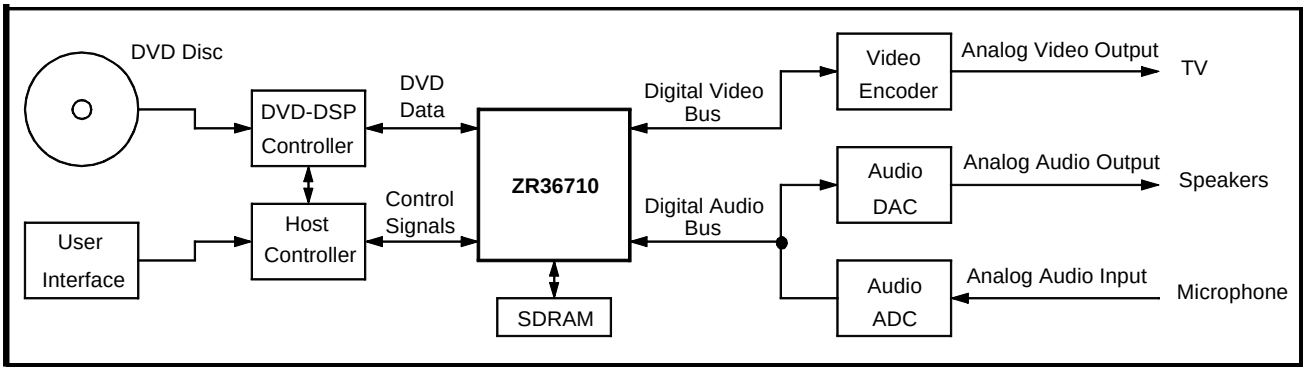

FIGURE 1. Simplified block diagram of the **ZR36710** in a stand-alone player.

Figure 1 shows a simplified block diagram of how the **ZR36710** is used in a stand-alone DVD player. The **ZR36710** is a single chip solution for decoding and presentation of the following types of data: DVD, VideoCD, CD-I (FMV), CD-DA, MPEG-2 (program) or MPEG-1 system multiplexed bitstreams, elementary streams, PES and stereo PCM audio. Where applicable, the **ZR36710** performs the following primary functions:

- Interpretation and execution of host commands that control the decoding/presentation (e.g. start, stop, pause, single-step, fast-forward).
- Acquisition of data, performing decryption (with authentication if necessary) on encrypted DVD content.
- Demultiplexing of video, audio, sub-picture, navigation packs and user data.
- Decoding of user-selected video, audio and sub-picture streams for post-processing prior to presentation.
- Synchronization of audio and video presentation (A/V sync) including proper execution and synchronization of sub-picture commands.
- NTSC <-> PAL conversion.
- Display aspect ratio (e.g. Letterbox or Pan-scan) video-post processing.
- Insertion of sub-picture Highlight information (HLI) and line 21 closed-caption data onto the video.
- Insertion of user-defined on-screen display (OSD) image overlay onto the video.
- Audio post processing, such as implementation of 3D audio algorithms.

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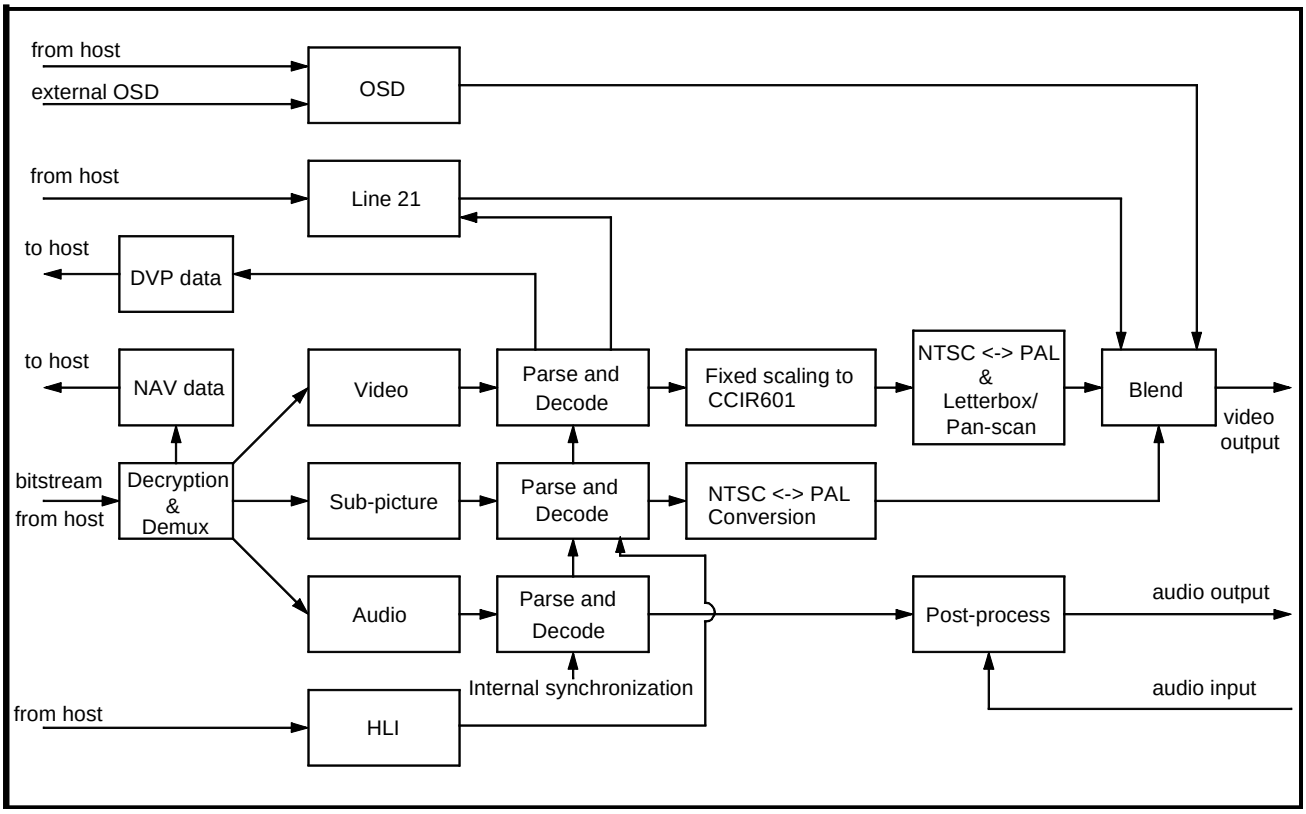

FIGURE 2. Simplified block diagram of the internal structure of the **ZR36710**.

The **ZR36710** requires one dedicated 1M*16-bit SDRAM (with an option for two SDRAMs if the user wishes to expand the functionality of the decoder which is not explained in the scope of this document). The SDRAM(s) is a -10 type (max clock rate of 100 MHz). The internal structure of the memory must be two banks of 2048 rows by 256 cells each.

The operation of the **ZR36710** is programmable via downloadable microcode and the writing of parameters to various registers. This allows for flexibility in the types of bitstreams the device can decode and support of bitstreams that may not necessarily adhere strictly to the MPEG-1, MPEG-2, DVD, AC-3, VideoCD, CD-i (FMV), and CD-DA specifications.

Figure 2 gives an overview of the internal architecture of the **ZR36710** with regards to the decoding functionality. Not shown is how each block may be configured via parameters or microcode, but these are explained in later sections. The following describes the key operations of the device.

Host Bus Interface and Host Commands

The primary interface between the host controller and the **ZR36710** is a parallel host bus that supports either an 8- or 16-bit data bus, a 4-bit address bus, an interrupt request line to generate interrupts to the host, and other host control signals. Two transfer I/O protocols (slave) are supported for either Intel- or Motorola-type transfers. Through the host bus the device is configured for decoding, issued control commands, provided with OSD data, queried for its current status and other functions required for proper operation of the device.

Host commands are issued to the device to control the playback mode. Aside from normal decoding/ playback of MPEG bitstreams, the following special modes are supported. In most of the special modes, the output of the audio is partially suspended. Audio output and synchronization with the video resume when normal playback operation is resumed.

- Pause Stream
- Single Stepping
- Slow Motion with slow-down (integer) factors of 2 to 7
- Fast Search
- Reverse Playback (for DVD content only, and 2 SDRAMs are required)
- End Playback

Some of these special modes are also applicable when playing back non-MPEG bitstreams or MPEG bitstreams without an active video stream.

Acquisition of Coded Data Including Decryption and Authentication of Encrypted DVD Content

The **ZR36710** provides three interfaces to the system for acquisition of bitstream data: A DVD-DSP (parallel) interface, a CD-DSP (serial) interface and a register of its host bus interface. The DVD-DSP and CD-DSP interfaces provide a glueless connection to several DVD drive controllers, simplifying the design of consumer DVD player applications. The host bus interface is targeted at applications in which data is provided via a VMI (Video Module Interface) Version 1.4 connector or similar interface.

The **ZR36710** performs decryption on encrypted DVD content. Authentication is also supported in a PC or any other environment in which authentication is a requirement.

Data provided via the DVD-DSP/CD-DSP interface must be in the following formats:

- **DVD data:** The **ZR36710** will request data from a DVD-DSP device in the form of 2048- to 2064-byte sectors. The maximum average rate for DVD content is 10.08 Mbits/sec. The sectors are either MPEG-2 data sectors or DVD navigation file (e.g. *.IFO or *.BUF files) sectors. The MPEG-2 data can include (as private streams) navigation packets, AC-3 coded multi-channel audio data, PCM audio data and sub-picture data. If the decoded audio is MPEG-1 or MPEG-2, Layer II is supported. The CD-DSP interface does not support DVD data.
- **VideoCD, CD-I, and CD-DA data:** 2352-byte sectors provided by the host at a constant bit rate (e.g. 1.411 Mbits/Sec). The sectors coming from the VideoCD or CD-I (FMV) discs are MPEG-1 data sectors (including data for CCIR high-resolution still images as well as SIF size), PCM audio data sectors (similar to CD-DA sectors) or auxiliary data sectors. If the decoded audio is MPEG-1, Layer II is supported. The sectors coming from CD-DA discs are 16 bits/channel stereo PCM data.

The bitstreams via the host bus interface can be either structured as sectors like those described above or as non-sector MPEG-2 (program) system-multiplexed bitstreams, MPEG-1 system-multiplexed bitstreams, elementary streams or graphics commands bitstreams.

Stream ID selection, Demultiplexing and Decoding

Stream IDs that select which audio, video and sub-picture stream are decoded can be switched both prior to decoding and during decoding. The **ZR36710** will demultiplex and decode the selected video, audio and sub-picture streams. Navigation packets (containing the PCI and DSI data), sequence headers, GOP headers, picture headers, and some of the user-data are parsed and stored within the **ZR36710** and its SDRAM to allow for host retrieval as necessary.

Audio/Video Synchronization

A/V sync (with proper sub-picture timing) is achieved by taking into account the relevant time stamps of the video, audio and sub-picture data and the actual delays of the reconstruction chains for each of these data types. Audio can be configured as the clock master and force all other bitstreams' decoding to synchronize to audio playback.

Display Aspect Ratio (e.g. Letterbox, Pan-scan) and NTSC <-> PAL Conversion

Prior to any aspect ratio or standards conversion, fixed scaling is performed on the decoded video. Each decoded image is scaled to CCIR size, 4:2:2 YUV (8 bits/component) as necessary (necessary if the decoded image is SIF size or "half D1" size, or for any size that is 4:2:0). Next, programmable scaling can scale the image from NTSC to PAL size or vice versa and also scale the image to a particular display aspect ratio to support display of 16:9 sources on 4:3 displays and vice versa (e.g. making use of "Letterbox" or "Pan-scan" methods). Scaling of sub-picture data is also performed as necessary depending on the output standard.

The video display frame rate is either 29.97 (NTSC) or 25 (PAL) frames per second. When necessary, automatic frame rate conversion is performed on coded MPEG-2 frame rates (or MPEG-1 picture rates, referred to as "frame" rates throughout the rest of this document) of 23.976, 25 or 29.97 per second. For example, for a display frame rate of 29.97 and coded frame rate of 23.976, automatic "3/2 pull down" is performed.

Insertion of Highlight (HLI) and Line 21 Closed-Caption Data

The HLI data for sub-picture "buttons" can be retrieved by the host when the **ZR36710** indicates that it has navigation packet data (The HLI data is part of the PCI portion of the navigation packet) available for host retrieval. The host can then write the HLI data to the appropriate registers within the device for proper sub-picture highlighting.

Closed-caption data can be automatically extracted from the GOP header data within the bitstream and inserted into the vertical blanking interval by the **ZR36710** without host intervention.

Insertion of On-Screen Display (OSD) Data

The host can overlay custom-graphics onto the video via the OSD feature. Pixel data is entered via the host bus and is represented by a 4-bit color index that specifies a 24-bit YUV color and one of four transparency levels. Each line of OSD has optional support for a "blinking" effect. The host determines on which lines the OSD begins and ends and which portion of the OSD memory is used for the actual display (allowing for scrolling effects). The **ZR36710** also supports keying of externally-generated OSD.

Video Output Interface

The **ZR36710** outputs the interlaced CCIR size, 4:2:2 YUV (8 bits/component) video frames at either NTSC or PAL rates on either an 8-bit (27 MHz VYUY format, with or without embedded SAV and EAV codes) or 16-bit (13.5 MHz YU/YV) pixel bus. The output of pixels on the video bus is synchronous with a video clock (either an input to or an output from the device) and contiguous along each video line, with ***HSYNC*** and ***VSYNC*** synchronization (sync) signals. The sync signals are either an input to the **ZR36710** or an output from the device, generated internally.

Image display "location" (relative to the sync signals) and size are defined by several set-up parameters. The size of the displayed part of the decoded image can be smaller than or equal to the size of the decoded image.

Audio Post-Processing and Output

Audio is output as 16-, 18-, 20- or 24-bit, two-channel PCM samples at 32, 44.1, 48 or 96 KHz with left and right samples interleaved on a serial bus according to the I^2S or EIAJ standards. Post-processing of the decoded audio and one stereo digital audio input, suitable for Karaoke and similar applications, is supported. Audio coded data or reconstructed data can be output on a single line using an internal

S/PDIF transmitter. When the source material is multi-channel audio, six (or eight) channel output (on three or four lines) is supported.

1.1 Feature List

- **Decoding**
  - Single chip solution for playback of DVD, VideoCD, CD-I (FMV), and CD-DA, and decoding of MPEG-1 (ISO 11172-1,2,3) or MPEG-2 (ISO 13818-1,2,3) system bitstreams including video, audio and synchronization of video and audio.
  - Decryption and authentication (if necessary) of encrypted DVD content.
  - Decoding and display of high resolution MPEG-1 still image sequences.
  - DOLBY-certified decoding of AC-3 multi-channel audio with optional down-mixing to two channels.
  - Decoding of MPEG-1 and MPEG-2 Layer II mono or stereo audio.
  - PCM audio playback from DVD, VideoCD, and CD-DA discs.
  - Decoding and playback of sub-picture (including Highlight), and closed captions ('line 21') data from DVD discs.
- **Display**
  - Interlaced video output.
  - NTSC and PAL standards. NTSC <-> PAL conversion.
- **Post Processing**
  - Karaoke mixing of decoded audio and two channels of input audio.
  - On-chip OSD engine with two 16-color (24-bit YUV) palettes, each with four levels of transparency; capability of blinking lines and vertical scrolling.
  - On-screen and off-screen OSD memory regions (dual-plane) for animation support.
  - Horizontal and vertical up- and down-scaling with bilinear vertical and horizontal interpolation.
  - Display aspect ratio conversion (16:9 <-> 4:3)
  - Automatic frame rate conversion (e.g. 3/2 pull down, NTSC <-> PAL frame rates).
  - EIA-608 compatible modulation of line 21 (NTSC) or line 22 (PAL) closed captions data over the video output.

- **Interfaces**
  - 8-bit CCIR 656 (with or without SAV and EAV information) or 16-bit CCIR 601 YUV 4:2:2 video output.
  - Externally or internally generated video sync signals and internally generated audio port clock signals.
  - 16/18/20/24-bit I^2S or EIAJ serial audio outputs.
  - 2 to 8 channels audio output.
  - S/PDIF output for compressed or (2 channel) reconstructed audio (according to IEC 958).
  - Dual protocol, dual width (8/16-bit) host interface.
  - Multiple-event, maskable interrupt request.
  - VMI 1.4 bus compliance.
  - Single 16-Mbit SDRAM (-10 speed) for all image sizes and formats.
  - Direct interface to DVD-ROM drive controllers via DVD-DSP or CD-DSP interface.
- **Miscellaneous**
  - Transfer to host of DVD navigation data, user data embedded in the MPEG video sequence, or navigation file sectors (VMGI, VTSI).
  - Block decoding and error correction of auxiliary data sectors (e.g. directories and play lists) of VideoCD discs.
  - Special operating modes: slow motion, fast search, etc.
  - On-chip PLL for maximum audio-video synchronization.
  - Picture-in-picture support.
  - Optional support for external OSD devices.
- **Physical Features**
  - Single 3.3 Volt supply.
  - 160 pin, TQFP package.
  - TTL I/O levels. Supports 5V input levels.
  - Single 27 MHz crystal/clock input.
  - 3-layer metal, 0.35 micron technology.
  - 1.0 W power consumption during operation.
  - < 90 mW power consumption during stand-by.

1.2 Typical Applications

- Stand-alone DVD players.
- DVD PC add-in cards.
- Digital broadcasting receivers (set-top boxes).

2. Notations and Conventions

2.1 Notations

- External signals: ***EXTERNAL, SIGNAL#, Y[7:0]***
- Internal variables, signals and status: **VARIABLE**, **SCLK**, **DVPVAL**, **STATUS0**
- Operating states: ***state, Idle***
- Active-low mark: #
- Configurable parameters: *FirstParameter, SecondParameter*
- Host commands: **host_command**, **start**
- Numbers:

  Unmarked numbers are decimal (e.g., 365, 23.19).

  Hexadecimal numbers are marked with a '0x' prefix (e.g., 0xB000, 0x3).

  Binary numbers are marked with a 'b' suffix (e.g., 010b, 0000110100011b).

  One-bit binary numbers (0 or 1) do not have the 'b' suffix.

- Math expressions: usually following the C syntax, except for the equality mark.

2.2 Definitions

- *Leading edge* of a signal, is the edge at the start of the active period of the signal. For active high signals, the leading edge is the rising edge. For active low signals the leading edge is the falling edge.
- *Trailing edge* of a signal, is the edge at the end of the active period of the signal. For active high signals, the trailing edge is the falling edge. For active low signals the trailing edge is the rising edge.
- *Set* and *reset* are used (as verbs) with the usual meaning according to the context. *Clear* is used also as a verb denoting setting of a binary value to 0.
- *Display frame* has the same meaning as in standard video. The display frame structure is interlaced; It is composed of two consecutive fields, Field I and Field II defined below.
- *Frame* (source, coded or reconstructed) can be either progressive or interlaced. The MPEG-1 standard specifies compression and decompression of a sequence of progressive frames only. The MPEG-2 standard specifies compression and decompression of a sequence of frames which can be either progressive or interlaced. Each frame (even a progressive frame) is divided into two fields, top field and bottom field as defined below. The pairing of the top and bottom fields with Field I and Field II can be selected once for a bitstream.
- *Picture* is the basic unit of a coded frame sequence. For MPEG-1, a picture contains the coded data of one (progressive) frame. Note that the notion of frame is not used in the MPEG-1 specs, and picture is synonymous with frame. For MPEG-2, each frame is coded either as a frame picture or as a pair of field pictures where one contains coded data of the top field and the other contains data of the bottom

field. Note that the order of the two field pictures in a frame needs not to be the same for different frames in the bitstream.

- *Format* (of a frame or of a picture) defines the number of color components, the color space, the relative horizontal and vertical size of the components (sub-sampling, or decimation), the relative location of the samples of the components and the representation (number of bits) of the samples of each component. The number of components for all formats defined in this specification is 3, the color space is Y, U and V, and the representation of each sample is 8 bits, unsigned integer.
    - *CCIR (4:2:2) format* - The U and V are decimated two-to-one horizontally. The U and V samples are situated with alternate Y samples (see Figure 3).
    - *MPEG-1 format* - The U and V are decimated two-to-one both horizontally and vertically. The U and V samples are situated in the middle between four Y samples (see Figure 4 and Figure 6).
    - *MPEG-2 format* - The U and V are decimated two-to-one both horizontally and vertically. The U and V samples are situated in the middle (vertically) between alternate pairs of Y samples (see Figure 5, Figure 7 and Figure 8).

- *Size* (of a frame or of a picture) is measured in the number of Y samples per line and number of Y-lines.
    - *SIF-NTSC size* is 240 lines by 352 pixels. For example, a SIF-NTSC size picture in MPEG-1 or MPEG-2 format has 240 lines by 352 samples/line of Y and 120 lines by 176 samples/line of U and V.
    - *SIF-PAL size* is 288 lines by 352 pixels. For example, a SIF-PAL size picture in MPEG-1 or MPEG-2 format has 288 lines by 352 samples/line of Y and 144 lines by 176 samples/line of U and V.
    - *Half D1-NTSC size* is 480 lines by 352 pixels. For example, a Half D1-NTSC size picture in MPEG-2 format has 480 lines by 352 samples/line of Y and 240 lines by 176 samples/line of U and V.
    - *Half D1-PAL size* is 576 lines by 352 pixels. For example, a Half D1-PAL size picture MPEG-2 format has 576 lines by 352 samples/line of Y and 288 lines by 176 samples/line of U and V.
    - *CCIR-NTSC size* is 480 lines by 704 (or 720) pixels.
    - *CCIR-PAL size* is 576 lines by 704 (or 720) pixels.

- *Field I* and *Field II*: Since an interlaced display frame has, usually, an odd number of lines, there is a difference in the arrangement of synchronization signals of two consecutive fields. The field which starts with the Vertical Synchronization (***VSYNC***) signal which is activated in the “middle” of the line, between two consecutive Horizontal Synchronization signals (***HSYNC***s) is designated Field II. The other field is designated Field I.
- *Top field* and *bottom field*: The display frame is divided into two fields of alternating lines. The field that includes the top line is designated the top field. The other field is called the bottom field.
- The input to the decoder is a bitstream. The bitstream is either an MPEG-1 system multiplexed bitstream, an MPEG-2 system multiplexed bitstream or a PCM audio bitstream. An MPEG system multiplexed bitstream includes several types of (elementary) streams (video, audio, private1, private2 and padding). A video stream within an MPEG system multiplexed bitstream includes the coded data

for one or more video sequences. A video sequence includes one or more pictures. An audio stream within an MPEG system multiplexed bitstream includes the coded data for one or more audio frames.

- RESET - The interval between activation and de-activation of the ***RESET#*** signal provided that it is longer than 160 ***GCLK*** periods. Also, the act of activating the ***RESET#*** signal for at least 160 ***GCLK*** periods and then de-activating the signal.
- STNDBY - The interval between activation and de-activation of the ***STNDBY#*** signal.
- Word - Two bytes unless specified otherwise.

2.3 Specifications

- VideoCD specs - White book, version 2.0 dated July 1994.
- CD-I (FMV) specs - Green book, dated March 1993, Chapter IX.
- DVD specs - Version 1.0, dated August 1996, and Supplemental Information, dated December 1996.
- Dolby AC-3 specs - ATSC DOC A-52, dated December 1995.
- Dolby AC-3 Licensing Manual, Version 1.0, dated October 1995.
- Line 21 (closed captions) specs - EIA-608, dated October 1994.
- S/PDIF specs - IEC 958, Digital audio interface, 1989.
- Video Module Interface specs - VMI Version 1.4.
- Video Interface Port specs - VIP Version 1.1, dated January 1997.

2.4 Acronyms

- m.s. - most significant.
- l.s. - least significant.
- ADP - The “Audio Data Processor” unit[1] within the **ZR36710**.
- DVP - The “Demultiplexer and Video Processor” unit[2] within the **ZR36710**.

1. The ADP consists of the audio “Parse and Decode” and “Post-process” blocks shown in Figure 2. The functionality of the ADP is configurable through dedicated ADP microcode, ADP commands and host commands as explained throughout this document.
2. The DVP consists of the video “Decryption & Demux” and “Parse and Decode” blocks shown in Figure 2. The functionality of the DVP is configurable through dedicated DVP microcode, set-up parameters and host commands as explained throughout this document.

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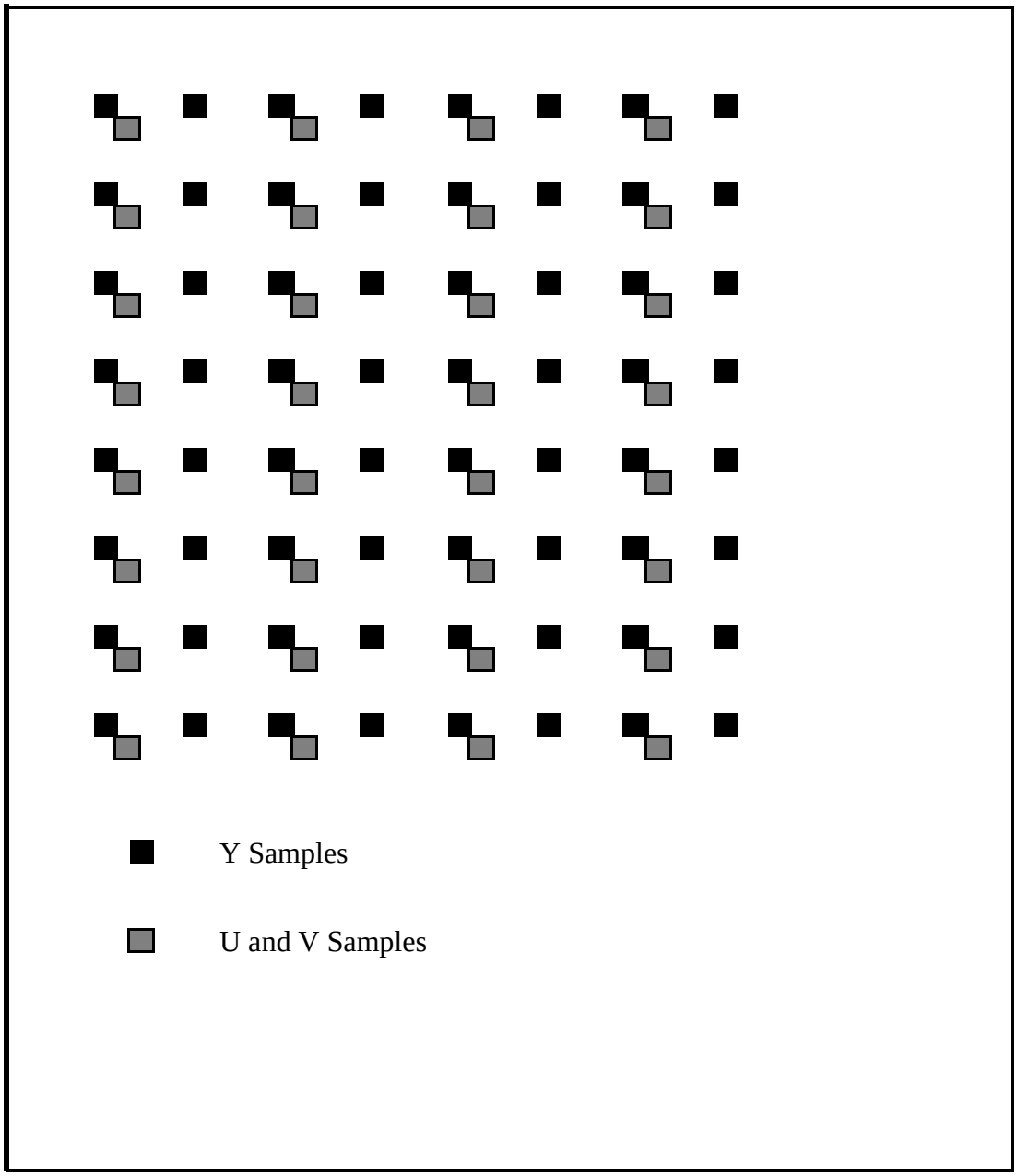

FIGURE 3. CCIR size, 4:2:2 format

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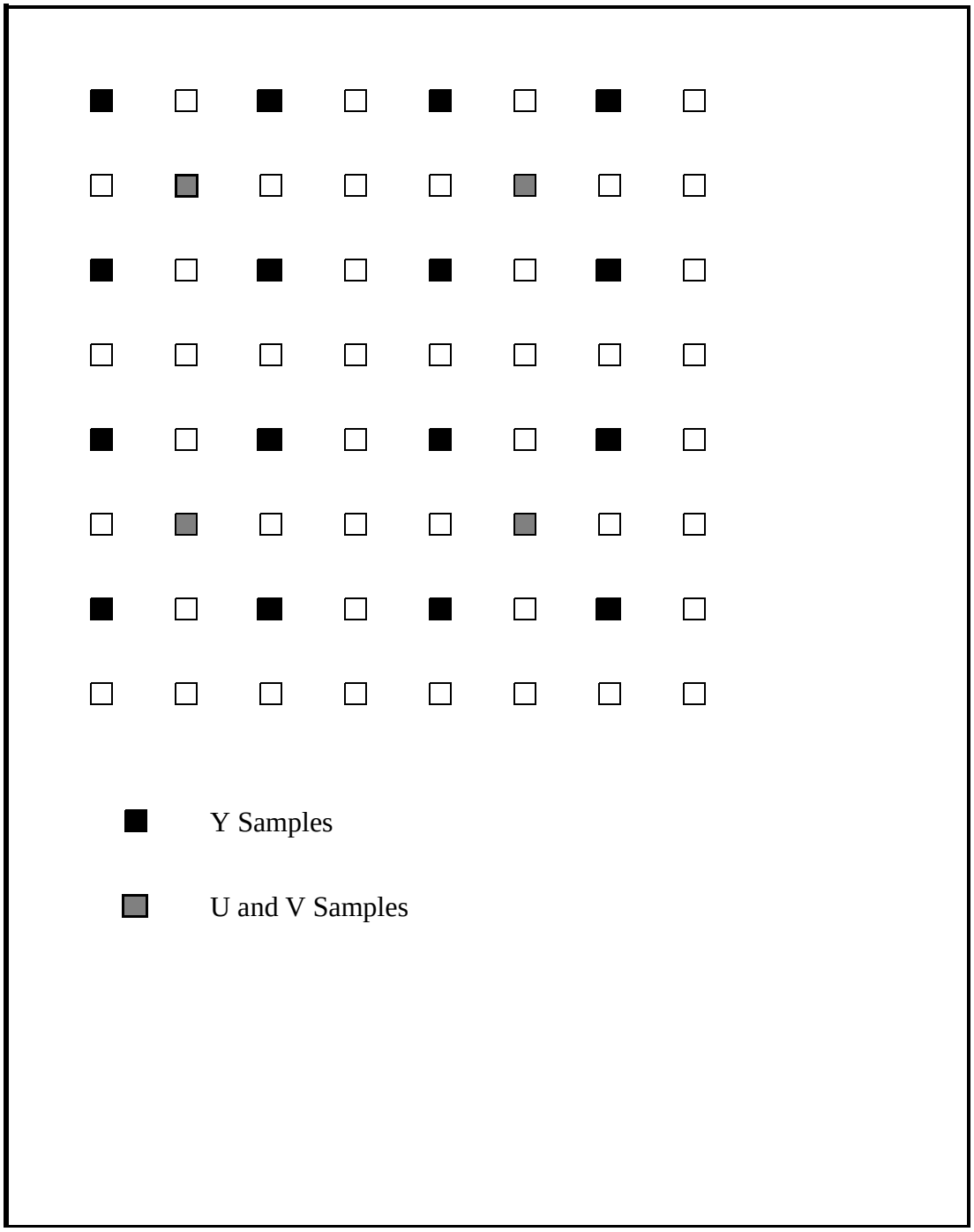

FIGURE 4. SIF size, MPEG-1 format, on CCIR size grid

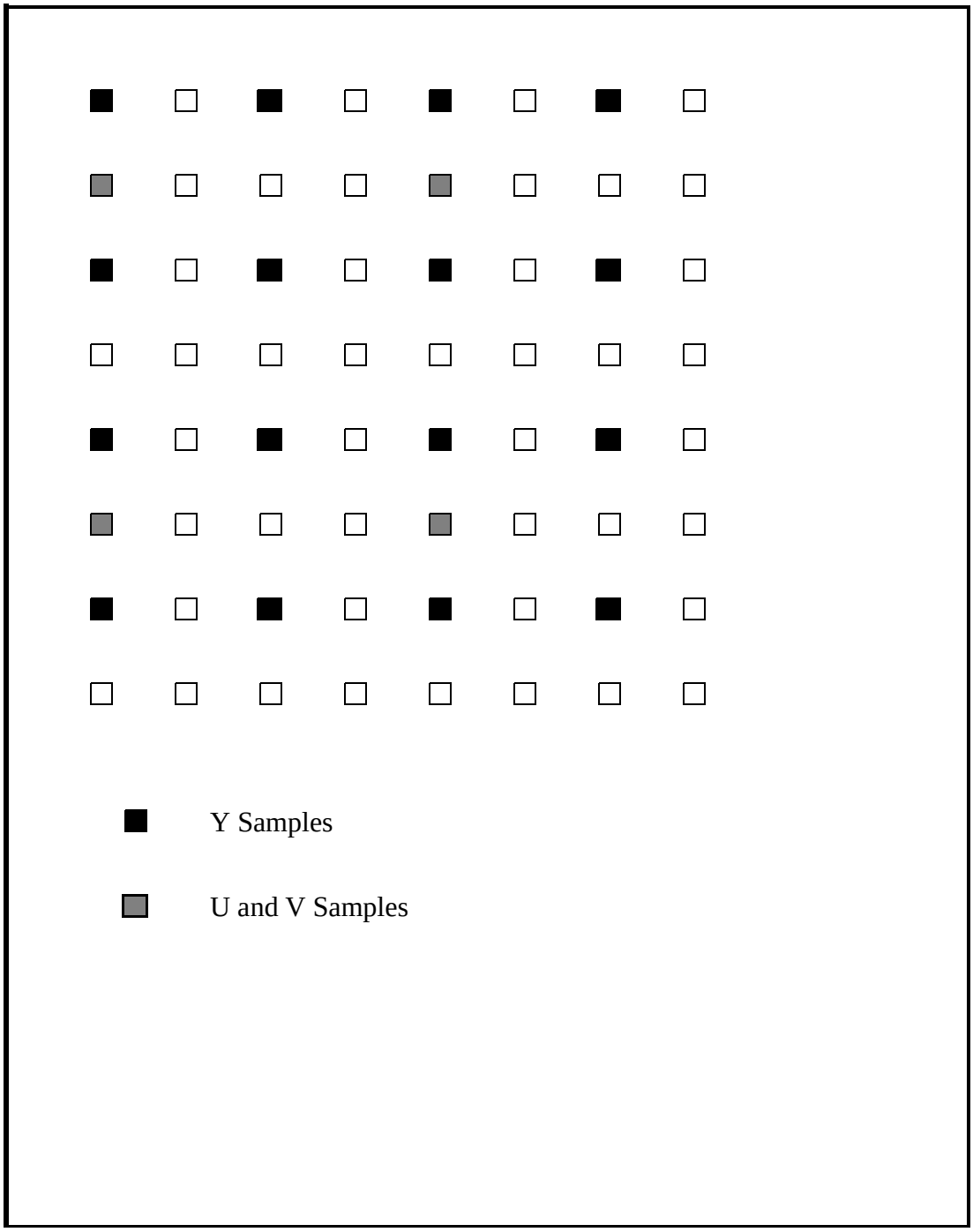

FIGURE 5. SIF size, MPEG-2 format, on CCIR size grid

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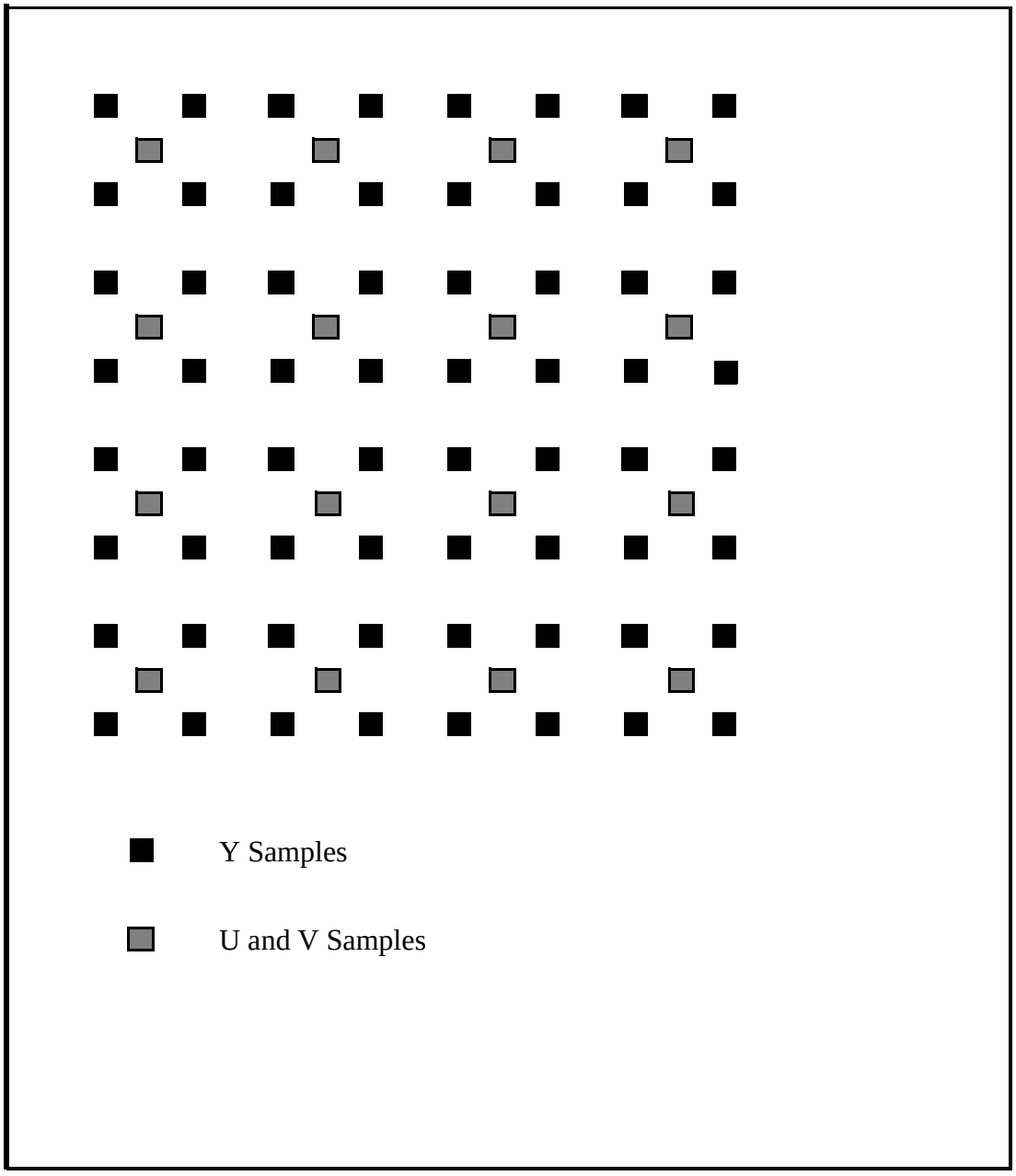

FIGURE 6. CCIR size, MPEG-1 format

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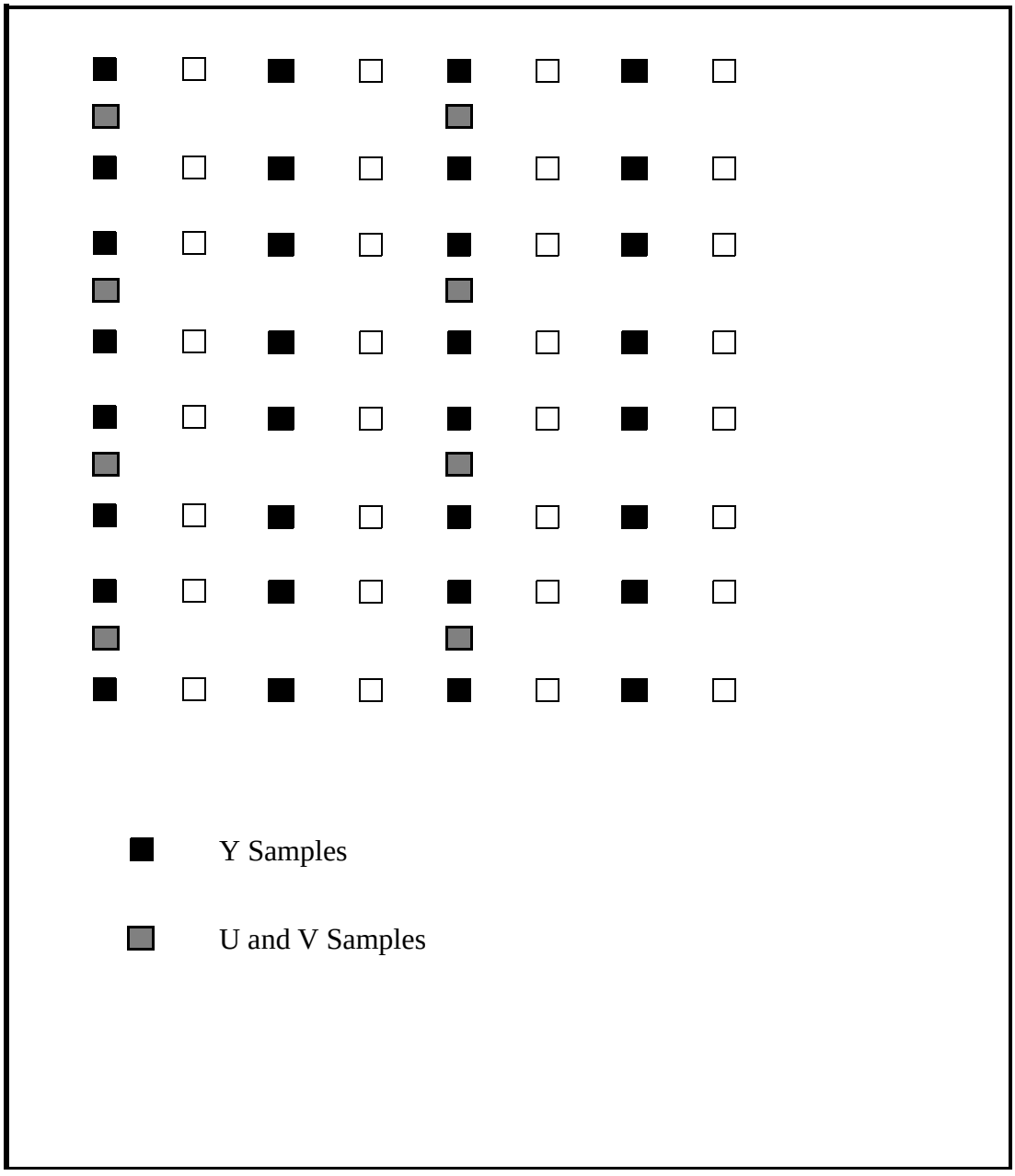

FIGURE 7. Half D1 size, MPEG-2 format, on CCIR grid

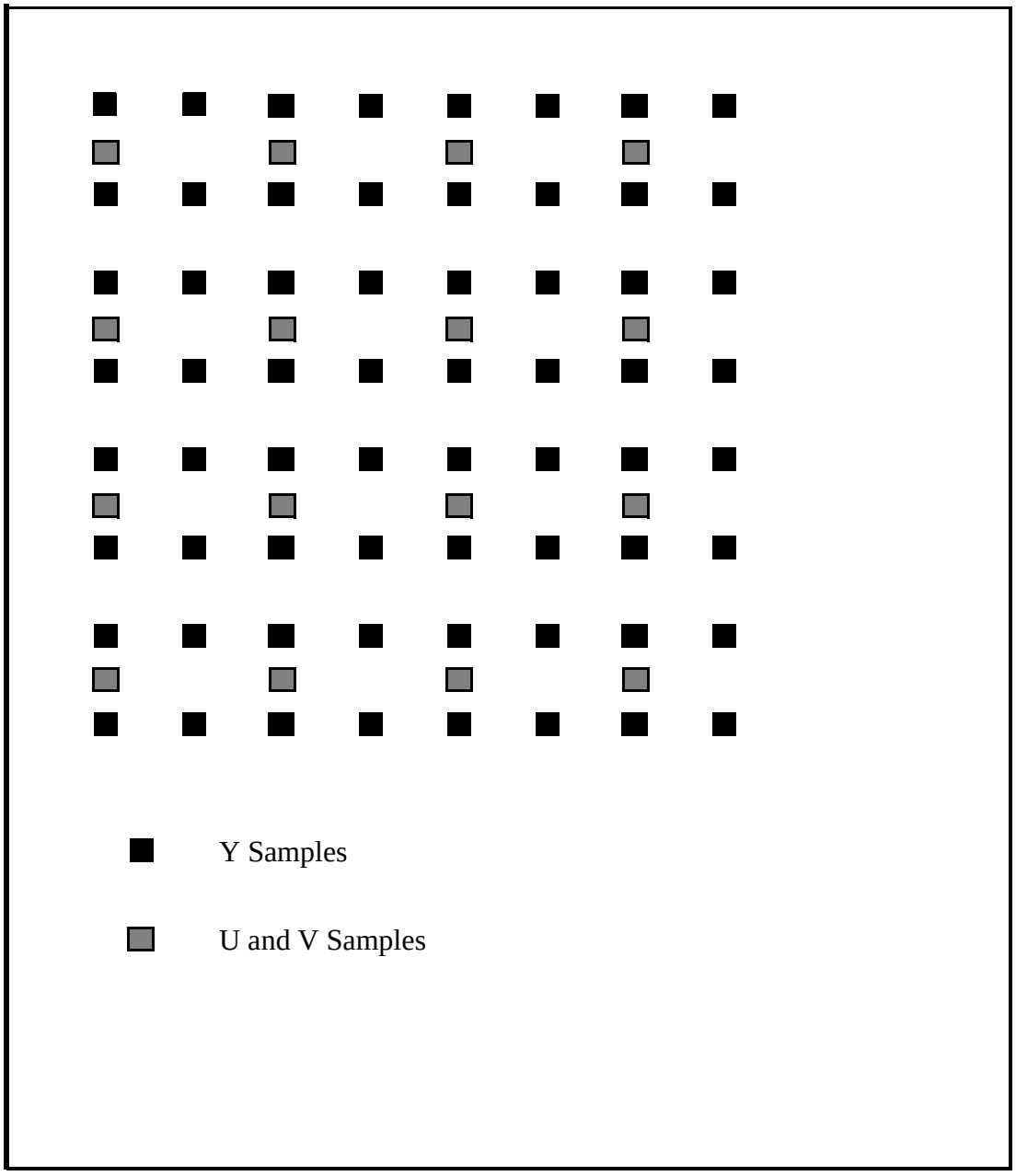

FIGURE 8. CCIR size, MPEG-2 format

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3. Pin Description

The **ZR36710** has 160 pins: 121 functional signals, 3 test signals, and 35 power signals (see the following figures). The table below lists the pins and their functions. Note that some of the functional pins may have a second function dedicated for testing which is not described here. Following is the table legend:

I - standard input-only. **O** - standard active driver. **3-S** - bi-directional I/O pin, with a 3-state option.

TABLE 1. **ZR36710** Pin Description

Symbol	Type	Direction	Description
Host Interface and CD-DSP Interface (32 pins)			
RESET#	I	I	Reset input (active low). Once de-asserted, the **ZR36710** initialization process begins.
STNDBY#	I	I	Stand-by input (active low). When asserted together with ***RESET#***, all outputs and bidirectional pins float, such that the **ZR36710** is electrically disconnected from its surroundings. All internal clocks are disabled, and the power consumption is minimized.
IDLE	3-S	O	***reset***, ***init_pclk***, ***init_display*** and ***Idle*** state indication output (active high).
HWID	I	I	Determines the width of the host interface data bus. It is allowed to be changed only during RESET. A low level (GND) configures the **ZR36710** to 8-bit host interface, a high level (V_{DD}) to 16-bit width.
HORD	I	I	Determines the order of bytes on the host interface data bus in the case of 16-bit width (***HWID*** at V_{DD}). It is allowed to be changed only during RESET. A low level (GND) configures the **ZR36710** to input/output the m.s. byte on ***HD[15:8]***, a high level (V_{DD}) to input/output the m.s. byte on ***HD[7:0]***. If ***HWID*** is at GND level, connect to GND.
HTYPE	I	I	Determines the protocol of the host bus. Can be changed only during RESET. A low level (GND) sets the **ZR36710** to Type A[a], a high level (V_{DD}) to Type B[a].
HD[7:0]	3-S	I/O	8 l.s. data lines of host data bus. When the ***HWID*** input is connected to GND, only these 8 l.s. signals are defined as host data signals. When ***HWID*** is connected to V_{DD}, these are the 8 l.s. lines of the 16-bit bus.
HD[11:8]	3-S	I/O	When ***HWID*** is tied to V_{DD}, these are data lines 11:8 of the 16-bit host data bus. When ***HWID*** is tied to GND, these are reserved pins.
HD[15:12]	3-S	I/O	When ***HWID*** is tied to V_{DD}, these are data lines 15:12 of the 16-bit host data bus. When ***HWID*** is tied to GND, these are the CD-DSP serial input port pins, defined as follows:
CDCLK (HD[12])	I	I	CD-DSP bit clock input
CDDAT (HD[13])	I	I	CD-DSP data input
CDFRM (HD[14])	I	I	CD-DSP left/right channel frame input

TABLE 1. **ZR36710** Pin Description

Symbol	Type	Direction	Description
Host Interface and CD-DSP Interface (32 pins)...continued.			
HA[3:0]	I	I	Host address inputs. These input signals indicate the register accessed in every cycle on the host interface.
HCS#	I	I	Host chip-select input. Active low.
HWR# (HR/W#)	I	I	In host protocol Type A[a] (***HTYPE*** = GND): ***HR/W#***. This input determines the direction of the host access. In host protocol Type B[a] (***HTYPE*** = V_{DD}): ***HWR#***. Host write input (active low).
HRD# (HDS#)	I	I	In host protocol Type A[a] (***HTYPE*** = GND): ***HDS#***. Data strobe input (active low). In host protocol Type B[a] (***HTYPE*** = V_{DD}): ***HRD#***. Host read input (active low.)
HRDY	3-S	O	Host ready output (active high). When this signal is high, up to *CodBurstLen*[b] bytes of bitstream can be written to the **ZR36710** with no need to poll its condition in between. When ***HRDY*** is deactivated during a host access, the host may write up to two additional bytes of bitstream without corrupting the data. When this signal is active, it is 3-stated (needs external pull-up resistor).
HIRQ#	3-S	O	Interrupt request (active low). This output signal requests an interrupt from the host controller. It is de-asserted if the host reads the interrupt status register, disables the interrupt, or toggles the **ZR36710** in and out of RESET. When this signal is not active, it is 3-stated (needs external pull-up resistor).
HACK#	3-S	O	Host acknowledge output (active low). In protocol Type A[a], the **ZR36710** indicates that a read or write cycle is completed by asserting this output. In protocol Type B[a], this signal is used by the **ZR36710** to indicate a “wait” state that may be used by “fast” hosts. In protocol Type B the host may ignore the ***HACK#*** signal. When this signal is not active, it is 3-stated (needs external pull-up resistor).
GPI/O Signals (4 pins)			
GPAI/O[1:0]	3-S	I/O	General purpose input/output pins, monitored/controlled by the ADP microcode. After RESET, these pins are defined as inputs. Their definition can be configured through ADP commands.
GPSI	I	I	General purpose input, monitored by the DVP microcode.
GPSO	O	O	General purpose output, controlled by the DVP microcode.
PLL Signals (6 pins)			
GCLK	I	I	27.000MHz clock or crystal input for main processing clock generation.
GCLK1	I	I	27.000MHz clock input for audio master clock generation. In normal operation must be connected to ***GCLK***.
XO	O	O	Output to a crystal that is connected to ***GCLK***. If a crystal is not used at ***GCLK***, ***XO*** must be left not connected.
PLLCA			PLL Capacitor. In normal operation must be connected to ***PLLGND*** through a 47nF capacitor.
PLLCFG[1:0]	I	I	PLL configuration inputs. Allowed to be changed only during RESET. In normal operation both pins must be connected to (digital) ***GND***.

TABLE 1. **ZR36710** Pin Description

Symbol	Type	Direction	Description
Digital Video Port (24pins)			
Y[7:0]	3-S	O	In 16-bit video mode (*Video8*[b] = 0) these lines are the luminance outputs. In 8-bit mode (*Video8* = 1) they are luminance/chrominance outputs, multiplexed in time according to the CCIR656 standard (with or without SAV and EAV sync codes).
C[7:0]	3-S	I/O	In 16-bit video mode (*Video8*[b] = 0) these lines are the chrominance outputs. In 8-bit mode (*Video8* = 1) the 3 m.s. lines (***C[7:5]***) are not used, and the 5 l.s. lines (***C[4:0]***) are defined as possible inputs from an external OSD device:
OSDPEL[3:0] (C[3:0])			OSD pixel value inputs. These four signals are sampled and used as an entry to an on-chip OSD palette.
OSDPLT (C[4])			On-chip OSD palette selector. A low level selects *OSDPalette0*[b], a high level selects *OSDPalette1*[b].
VCLKx2	3-S	I/O	Main video clock input or output. 27.000MHz.
VCLK	3-S	I/O	A division by two of the ***VCLKx2*** signal. This signal is used as data and sync qualifier.
HSYNC	3-S	I/O	Horizontal sync input/output. Polarity and duration are programmable.
VSYNC	3-S	I/O	Vertical sync input/output. Polarity and duration are programmable.
FI	3-S	I/O	Field indication input/output. Polarity is programmable.
CBLANK	O	O	Composite blank output. Waveform, including polarity, is programmable.
VMASTER	I	I	Video master/slave selection input. When this input is high, the **ZR36710** is the video sync master (video SYNC signals and clocks are output). When it is low, the **ZR36710** is a video Sync slave (video SYNC signals and clocks are input). This input may be changed only during RESET.
VDEN#	I	I	Video enable input (active low). When this input is active, the **ZR36710** may output video data. When it is deasserted, the **ZR36710** 3-states the pixel outputs (although the sync signals and clocks are still active). This input may be changed at any time, taking effect at the next ***VCLKx2***.
Digital Audio Port (8 pins)			
AMCLK	3-S	I/O	Audio Master Clock input/output. 384, 256, 192 or 128 times the sampling frequency (programmable).
S/PDIF (AOUT[3])	O	O	S/PDIF transmitter output for digital coded or reconstructed audio data. Alternately can be used as a fourth audio output. After RESET this pin outputs low level.
AOUT[2:0]	O	O	Audio serial data output lines, 2 channels per line. After RESET these pins output low level until audio playback is performed.
AIN	I	I	Serial input of digital stereo audio.
ALRCLK	O	O	Digital audio left/right select output for the audio port. Square wave, at the sampling frequency. Programmable polarity interpretation for input and output.
ABCLK	O	O	Digital audio bit-clock output. Data on ***AOUT*** and ***AIN*** is output or latched, respectively, with the rising or falling edge of this clock. Data on ***AOUT*** and ***AIN*** can be latched on different edges of ***ABCLK***.

TABLE 1. **ZR36710** Pin Description

Symbol	Type	Direction	Description
DVD-DSP Interface (12 pins)			
DVDREQ	O	O	DVD-DSP data request output. Programmable polarity.
DVDVALID	I	I	DVD-DSP data valid input. Programmable polarity.
DVDSOS	I	I	DVD-DSP start of sector input. Programmable polarity.
DVDDAT[7:0]	I	I	DVD-DSP data input bus.
DVDSTRB	I	I	DVD-DSP data bit strobe (clock) input. Programmable polarity.
SDRAM Interface (35 pins)			
RAMDAT[15:0]	3-S	I/O	SDRAM bidirectional data bus.
RAMADD[11:0]	O	O	SDRAM address bus output.
RAMRAS#	O	O	SDRAM row select (active low) output.
RAMCAS#	O	O	SDRAM column select (active low) output.
PCLK	O	O	SDRAM clock output (Same as internal processing clock).
RAMDQM	O	O	SDRAM data masking (active high) output.
RAMCS0#	O	O	SDRAM chip select (active low) output for the lower 2MByte device.
RAMCS1#	O	O	SDRAM chip select (active low) output for the upper 2MByte device.
RAMWE#	O	O	SDRAM write enable (active low) output.
Test Signals (3 pins)			
SCNENBL	I	I	In normal operation this pin must be connected directly to GND.
TESTMODE	I	I	In normal operation this pin must be connected directly to V_{DD}.
ICEMODE	I	I	In normal operation this pin must be connected directly to V_{DD}.
Power Signals (35 pins)			
GND	ground		Digital ground.
V_{DD}	power		Digital power supply (3.3V).
PLLGND	ground		Ground plane of internal PLL circuit.
$PLLV_{DD}$	power		Power supply for internal PLL circuit (3.3V).

a. See Section 4.3.2 “Protocol of Host Transfers - HTYPE” for an explanation on Type A and B host bus protocols.

b. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”for an explanation on loading set-up parameters to the **ZR36710**.

Pin assignment and signal status during RESET, STNDBY and after RESET are described in Section 13. “Annex B: Pin Assignment and Signal Status”.

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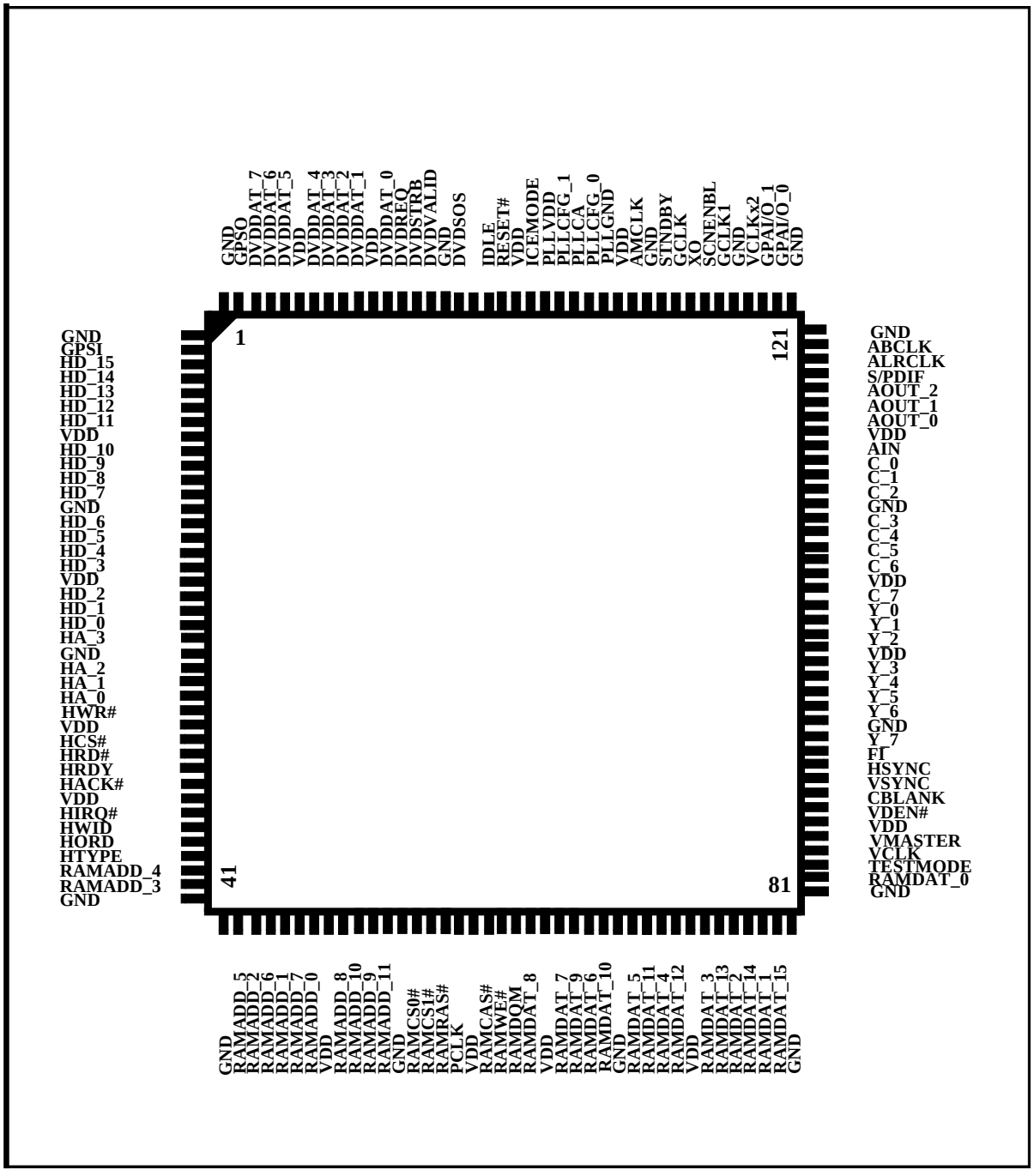

FIGURE 9. Pinout Diagram

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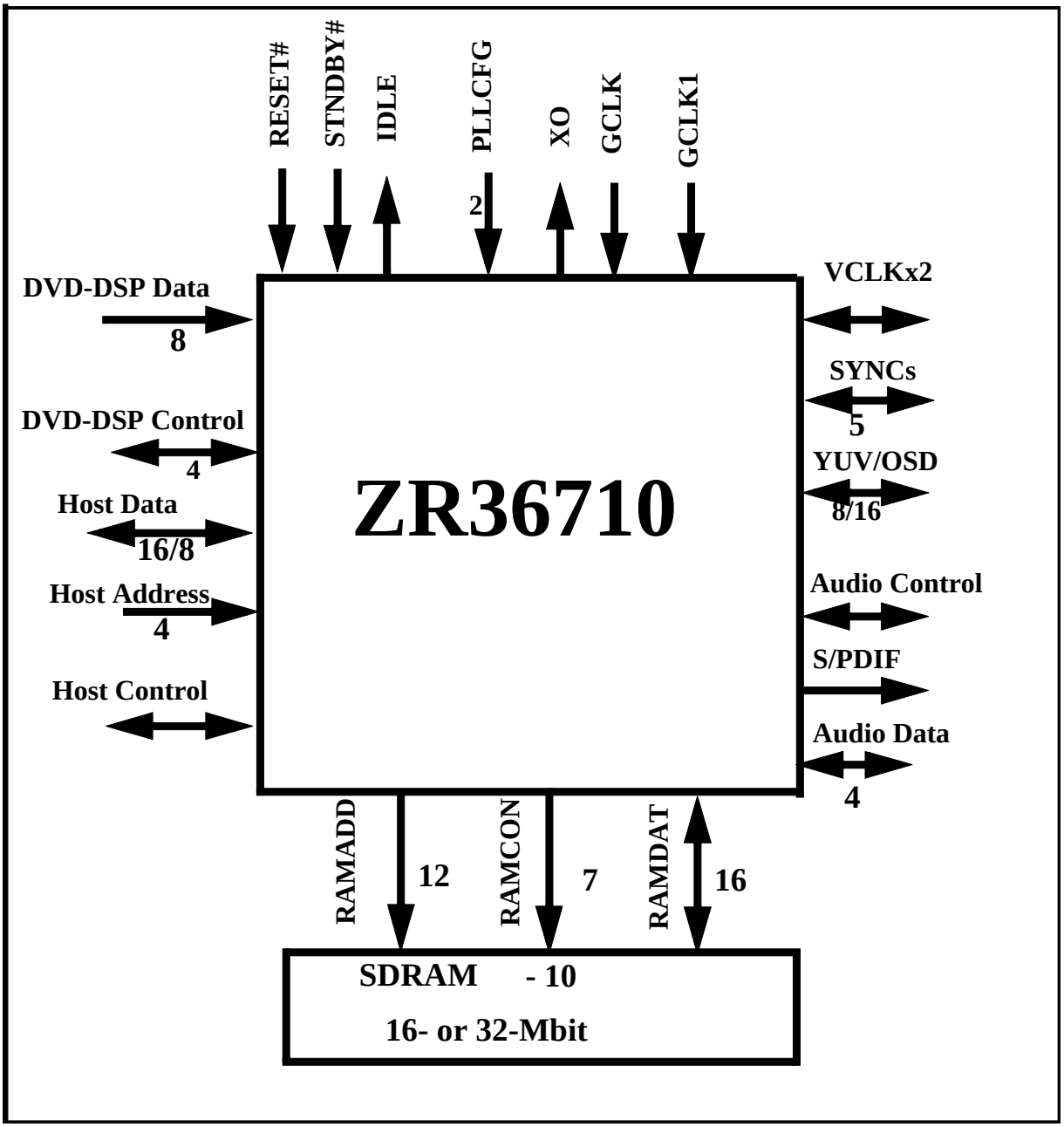

FIGURE 10. External Interface Signals

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4. Hardware Interfaces

Table 1 shows that the pins of the **ZR36710** are grouped into various interfaces. These interfaces are grouped as follows:

- SDRAM interface.
- Phase-locked loop interface.
- Host bus interface.
- DVD-DSP and CD-DSP interfaces.
- Video bus interface.
- Audio bus interface.

This section explains these interfaces.

4.1 SDRAM Interface

The SDRAM interface consists of:

- 16-bit bidirectional data bus ***RAMDAT[15:0]***
- 12-bit address bus ***RAMADD[11:0]***
- one clock output line ***PCLK***
- 6-signal output control bus ***RAMDQM***, ***RAMCS0#***, ***RAMCS1#***, ***RAMRAS#, RAMCAS#*** and ***RAMWE#***

The write and read operations are in the “fast page” mode. The **ZR36710** indicates a write operation by activating the ***RAMWE#*** signal, otherwise the operation is read. The ***CKE*** line of the SDRAM devices should be connected to $\mathbf{V_{DD}}$. Refresh operations are also handled by the device.

The *NumDRAMDev* bit in the *SysConfig*[1] set-up parameter allows the host to indicate to the **ZR36710** the number of 16M SDRAMs used by the device:

- *NumDRAMDev* = 0, One SDRAM.
- *NumDRAMDev* = 1, Two SDRAMs.

The detailed timing is given in Section 11. “DC and AC Characteristics”. The timing reflects the requirement for a “-10” type or faster SDRAM. The SDRAM’s internal structure must be two banks of 2048 rows by 256 cells each.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

4.2 Phase-Locked Loop Interface

The internal PLL circuitry of the **ZR36710** uses two clock signals (***GCLK*** and ***GCLK1***) to generate the following two primary clocks of the device, from which several other clocks (e.g. ***VCLK***, ***VCLKx2***) are derived:

- ***PCLK*** - 81 MHz SDRAM clock and internal processing clock for the **ZR36710**.
- ***AMCLK*** - 128, 192, 256 or 384f_s audio port clock, where f_s (the PCM audio sampling rate) is either 32, 44.1 or 48 KHz as encoded in the audio stream. Note that this clock is an input after RESET, but must be changed to an output as explained in Section 4.6 “Audio Interface”.

Table 2 shows the configuration of these two clocks. These clocks are configured via the PLLTAB and PLLCFG ADP commands[1] as shown in Table 2 . The *DSPM*[1] and *DSPD*[1] values of the PLLTAB command, along with ***GCLK***, must guarantee a ***PCLK*** of 81 MHz. If ***GCLK*** = 27 MHz, the default values of *DSPM* and *DSPD* will generate ***PCLK*** = 81 MHz and require no loading by the host.

The various combinations of *AUDM*[1], *AUDD*[1] and *SR*[1] values in the PLLTAB ADP command have default values after RESET for audio sampling rates of 32, 44.1 and 48 KHz for a 256f_s ***AMCLK*** if ***GCLK1*** = 27 MHz. *AUDM* and *AUDD* must be loaded by the host for *SR* = 3 (96 KHz).

Section 4.2.2 “Changing PLL Values” explains when these clocks can/must be changed.

TABLE 2. ***PCLK*** and ***AMCLK*** Configuration

Clock Pin	Equations	Restrictions
PCLK	***PCLK*** = ***GCLK*** x *DSPM* / *DSPD* ***GCLK*** = 27 MHz. ***PCLK*** = ***GCLK*** during RESET.	1 <= *DSPM* <= 255, 1 <= *DSPD* <= 63. 8 MHz <= ***GCLK*** <= 50 MHz. *DSPM* = 3 default after RESET. *DSPD* = 1 default after RESET.
AMCLK	f_s = 32.0KHz: ***AMCLK*** = ***GCLK1*** x *AUDM* / *AUDD*, *SR* = 2 f_s = 44.1KHz: ***AMCLK*** = ***GCLK1*** x *AUDM* / *AUDD*, *SR* = 1 f_s = 48.0KHz: ***AMCLK*** = ***GCLK1*** x *AUDM* / *AUDD*, *SR* = 0 f_s = 96.0KHz: ***AMCLK*** = ***GCLK1*** x *AUDM* / *AUDD*, *SR* = 3 ***GCLK1*** = 27 MHz (tied to ***GCLK***) is highly recommended. ***AMCLK*** = ***GCLK1*** / 4 during RESET. ***AMCLK*** = ***GCLK1*** x *AUDM* / *AUDD* for *SR* = 0 after RESET.	1 <= *AUDM*, *AUDD* <= 8191. 8 MHz <= ***GCLK1*** <= 50 MHz. *AUDM* and *AUDD* are automatically loaded after RESET for *SR* = 0, 1 and 2 for an ***AMCLK*** = 256f_s if ***GCLK1*** = 27 MHz.

The *SR*[1] value of the PLLCFG ADP command is used to select which set of *AUDM* and *AUDD* parameters are to be used. The values allowed are shown in Table 3 . After RESET, the *SR* = 0, selecting ***AMCLK*** = 256 x 48 KHz.

1. See Section 12.4 “Set-up Commands” for an explanation on changing the ***PCLK*** and ***AMCLK*** frequencies via the PLLCFG and PLLTAB ADP commands.

TABLE 3. Selection of Sampling Frequency and ***AMCLK*** via *SR* of the PLLCFG ADP Command

Value	Action
SR = 000b	The AUDM and AUDD values associated with a 48 KHz sampling rate are used (default after RESET).
SR = 001b	The AUDM and AUDD values associated with a 44.1 KHz sampling rate are used.
SR = 010b	The AUDM and AUDD values associated with a 32 KHz sampling rate are used.
SR = 011b	The AUDM and AUDD values associated with a 96 KHz sampling rate are used.
SR = 111b	Automatic selection as explained in Section 4.2.3 “Automatic Selection of AMCLK”.

Figure 11 shows the recommended hardware configuration for both crystal (first and third overtone crystals) and TTL clock sources for ***GCLK*** and ***GCLK1***. These clocks must be phase-locked for proper operation of the device. A single clock source of 27 MHz is recommended.

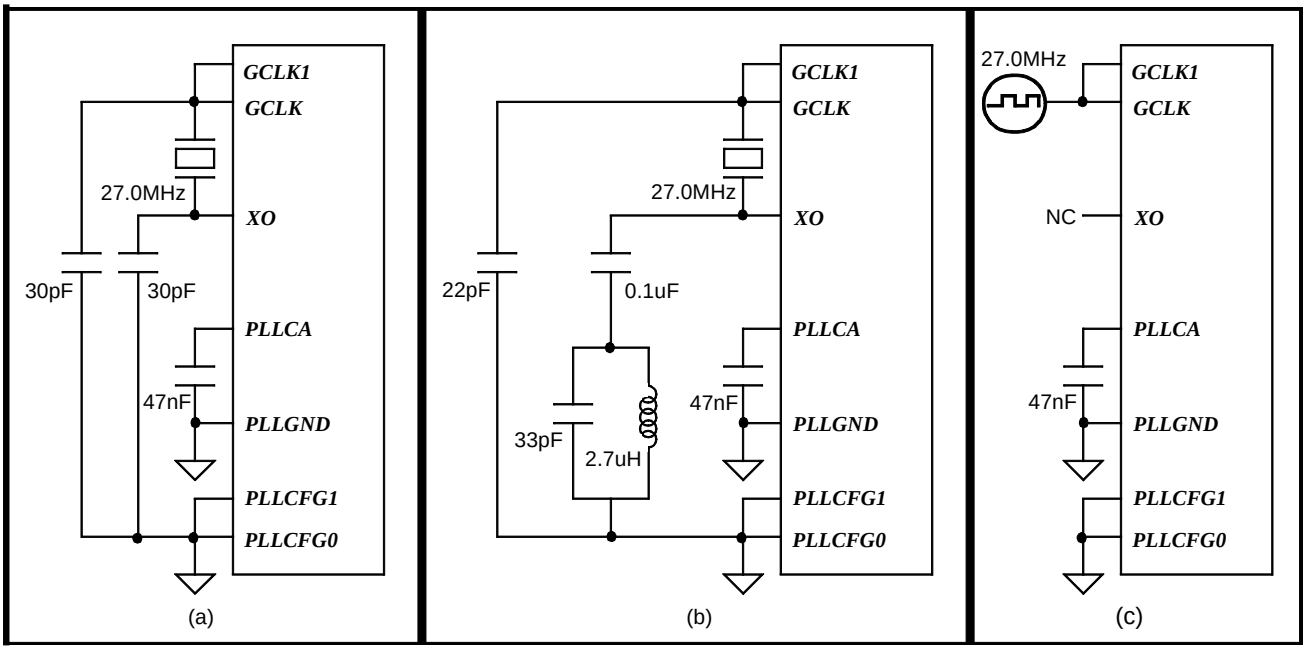

FIGURE 11. PLL Interface in normal operation, with a first harmonic crystal (a), with a third overtone crystal (b) and with a clock (c). The crystal is parallel resonant.

4.2.1 PLL Initialization after RESET

Table 2 shows the values of ***PCLK*** and ***AMCLK*** during and after RESET, but there is a latency between disabling RESET and when the PLL locks to these frequencies. This latency is reflected by the status of

the **PLLpLOCKED** and **PLLaLOCKED** bits of the Interrupt Status Register, or ISR[1], as shown in Table 4 . The **C-STATE** bits of the **STATUS0**[2] register also reflect the latency of locking ***PCLK***.

TABLE 4. ***PCLK*** and ***AMCLK*** Locking after RESET

Clock Pin	Unlocked	Locked
PCLK	**PLLpLOCKED** = 0 **C-STATE** = 00 0000b (***reset***)	**PLLpLOCKED** = 1 **C-STATE** = 00 0010b (***init_pclk***)
AMCLK	**PLLaLOCKED** = 0	**PLLaLOCKED** = 1

4.2.2 Changing PLL Values

Any of the following conditions would require a change to one or more of the *DSPM*, *DSPD*, *AUDM*, *AUDD* and *SR* values since their default values would be obsolete:

- ***GCLK*** is not 27 MHz (thus ***PCLK*** would not default to the required 81 MHz).
- ***GCLK1*** is not 27 MHz (thus ***AMCLK*** would not default to 256f_s).
- The external audio DAC(s) must use a sampling clock of 128f_s, 192f_s, or 384f_s rather than 256f_s.
- The sampling rate of the audio is not 48 KHz.

4.2.2.1 Changing *PCLK*

Changes to the *DSPM* and/or *DSPD* values should only be done once, immediately after RESET. The *DS* value of the PLLCFG ADP command must be set to 1 to initiate ***PCLK*** re-locking. Any changes will clear the **PLLpLOCKED** bit of the ISR temporarily while ***PCLK*** re-locks. Once ***PCLK*** is re-locked, the **PLLpLOCKED** bit will be set to 1.

4.2.2.2 Changing *AMCLK*

Changes to the *AUDM*, *AUDD* and/or *SR* values can be done at any time after RESET. The *AS* value of the PLLCFG ADP command must be set to 1 to initiate ***AMCLK*** re-locking (unless SR = 111b). Any changes will clear the **PLLaLOCKED** bit of the ISR temporarily while ***AMCLK*** re-locks. Once ***AMCLK*** is re-locked, the **PLLaLOCKED** bit will be set to 1.

If ***GCLK1*** = 27 MHz, ***AMCLK*** = 256f_s and f_s = 32, 44.1 or 48 KHz, only the *SR* value of the PLLCFG ADP command needs to be changed since default *AUDM* and *AUDD* values already exist for these sampling frequencies. No PLLTAB ADP command needs to be sent.

4.2.3 Automatic Selection of AMCLK

If *SR* = 111b (of the PLLCFG ADP command), the PLL circuitry will automatically select which set of *AUDM* and *AUDD* parameters to use, depending on the sampling rate of the audio data. If the device automatically switches between sets of values, **PLLaLOCKED** will be cleared for up to 50ms while the

1. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.
2. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

PLL re-locks ***AMCLK***. Once ***AMCLK*** is re-locked, **PLLaLOCKED** is set to 1. The *AS* value of the PLLCFG ADP command does not need to be set to 1 if automatic selection is used.

4.3 Host Bus Interface

The **ZR36710**'s host bus is the primary interface to the host controller through which the host controls and monitors the operation of the device. The host interface is designed for asynchronous operation. Features of the host interface include:

- Selectable 8-bit or 16-bit data bus with selectable byte-ordering for the 16-bit data bus.
- 4-bit address bus and single-line chip select that allows the host to communicate with 16 addressable 16-bit locations (either one 16-bit transfer or two 8-bit transfers, depending on the data bus width).
- Selectable transfer protocol - Type A or Type B.
- One IRQ line allows the **ZR36710** to interrupt the host controller on a number of events.
- A data request line that allows the **ZR36710** to request coded bitstream data from the host (if the DVD-DSP and CD-DSP interfaces are disabled).
- Two dedicated ADP I/O lines which may be used as general purpose I/O lines (if the ADP microcode allows such usage).
- Two dedicated DVP I/O lines, one for input and the other for output.

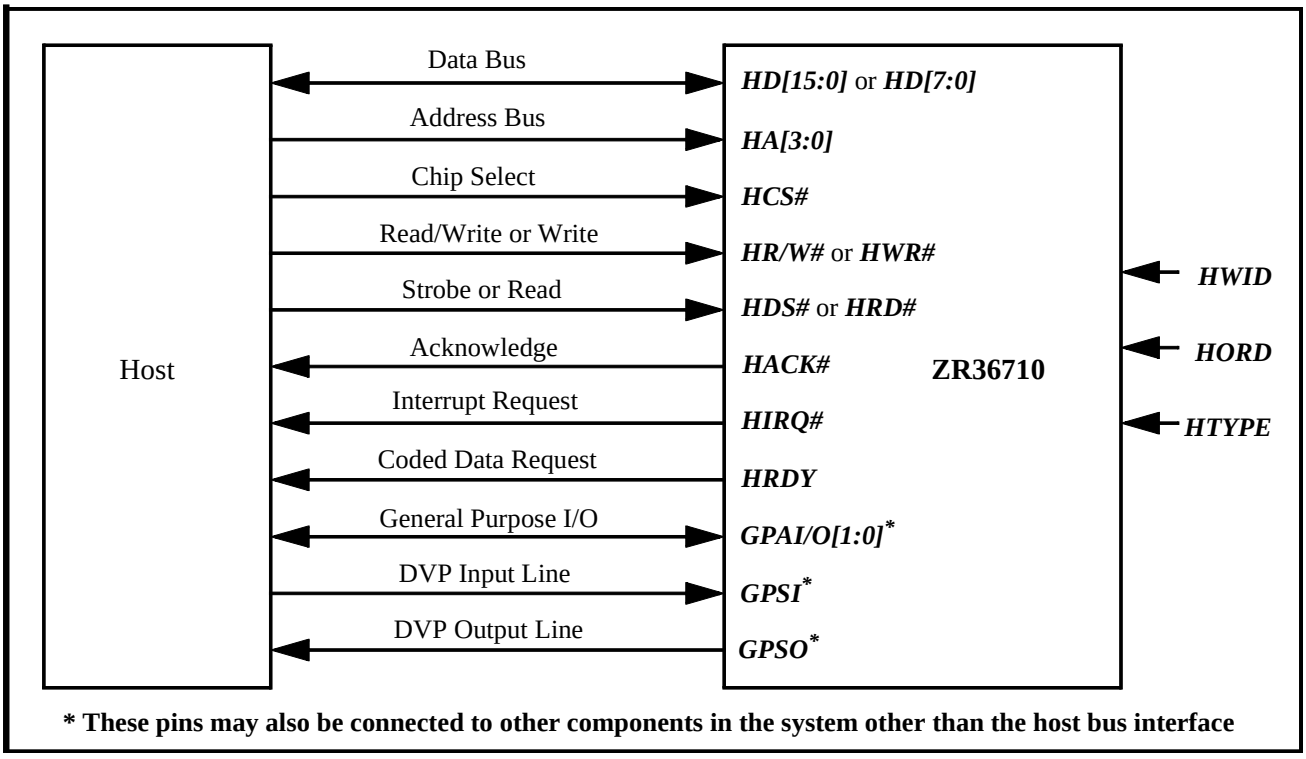

FIGURE 12. Host Interface Signals

4.3.1 Width and Byte Ordering of the Host Data Bus - *HWID* and *HORD*

The ***HWID*** and ***HORD*** pins select the data bus width and byte-ordering as shown in Table 5 .

TABLE 5. ***HWID*** and ***HORD*** Selection of Data Bus Width and Byte-Ordering

HWID	*HORD*	Data Bus Width and Byte-Ordering
GND	**GND**	8-bit data bus using only ***HD[7:0]***.
GND	**V_{DD}**	Illegal configuration. Do not use.
V_{DD}	**GND**	16-bit data bus, m.s. byte on ***HD[15:8]***, l.s. byte on ***HD[7:0]***.
V_{DD}	**V_{DD}**	16-bit data bus, m.s. byte on ***HD[7:0]***, l.s. byte on ***HD[15:8]***.

When the 8-bit mode is selected, the ***HD[15:8]*** signals are not used for the host bus and can be used for a serial CD-DSP interface (see Section 4.4.2 “CD-DSP Serial Data Interface”).

4.3.2 Protocol of Host Transfers - *HTYPE*

The **ZR36710** supports two types of host protocols, Type A and Type B. The valid protocol is determined by the ***HTYPE*** input pin. Pins 27 and 30 have dual-functionality that is dependent on the host protocol as shown in Table 6 .

TABLE 6. ***HTYPE*** and Functionality of Pins 27 and 30

HTYPE	Protocol	Pin Definition
GND	Type A	Pin 27 is ***HR/W#***. Pin 30 is ***HDS#***.
V_{DD}	Type B	Pin 27 is ***HWR#***. Pin 30 is ***HRD#***.

4.3.2.1 Host Protocol Type A

This protocol supports hosts that have a single read-write signal (direction selector) and a data strobe signal. It also complies with host interface Mode A of the VMI Specification Version 1.4. Figure 13 illustrates the timing of the Type A host-write and host-read cycles.

TABLE 7. Type A Transfers

Direction	Sequence of Type A Handshakes
Write	1. Host asserts ***HCS#***, ***HR/W#*** (low), selects an address on ***HA[3:0]*** and places data on ***HD*** lines. 2. Host asserts ***HDS#***, indicating to the **ZR36710** that data is valid. 3. **ZR36710** latches-in the data and then asserts ***HACK#*** in response to ***HDS#*** assertion. 4. Host de-asserts ***HDS#*** and ceases to drive the ***HD*** lines in response to ***HACK#*** assertion. 5. **ZR36710** de-asserts ***HACK#*** in response to ***HDS#*** de-assertion.
Read	1. Host asserts ***HCS#***, ***HR/W#*** (high) and selects an address on ***HA[3:0]***. 2. Host asserts ***HDS#***, indicating to the **ZR36710** that it requests data. 3. **ZR36710** places the data on the ***HD*** lines and then asserts ***HACK#*** in response to ***HDS#*** assertion. 4. Host de-asserts ***HDS#*** upon latching-in the data on the ***HD*** lines. 5. **ZR36710** de-asserts ***HACK#*** in response to ***HDS#*** de-assertion and ceases to drive the ***HD*** lines.

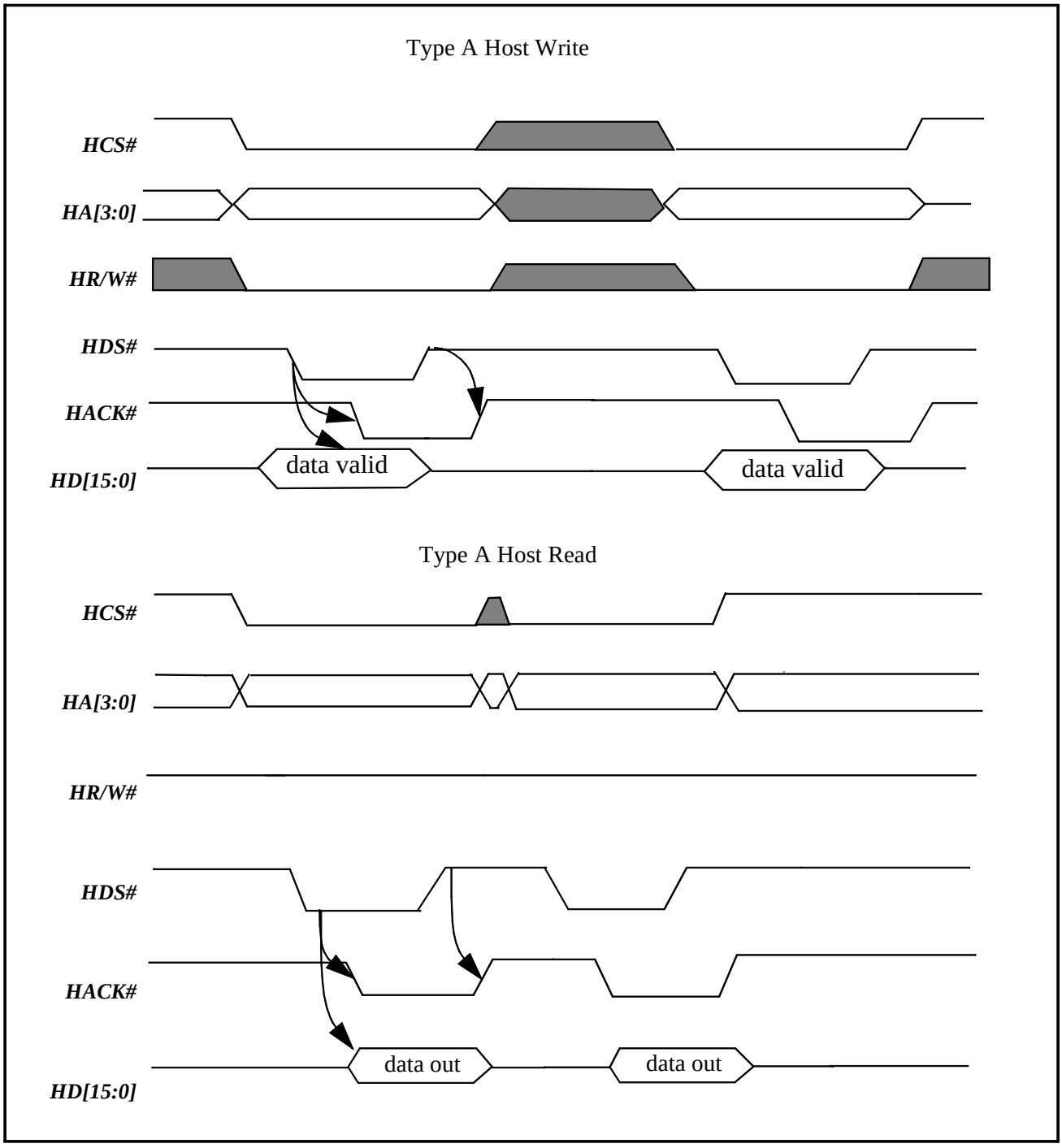

FIGURE 13. Host interface protocol -Type A. ***HD[15:0]*** can also be ***HD[7:0]*** for 8-bit interface.

4.3.2.2 Host Protocol Type B

This protocol supports hosts that have two separate signals for read and write and do not use a data strobe signal. It also complies with host interface mode B of the VMI Specification Version 1.4. Figure 14 illustrates the timing of the Type B host-write and host-read cycles.

The usage of ***HACK#*** in this mode is optional, depending on the timing of the host's ***HWR#*** and ***HRD#*** cycles:

- If the host ***HWR#*** and ***HRD#*** cycles meet the minimum duration according to the **ZR36710** timing, the host may ignore ***HACK#*** (which may be not connected).
- If the host ***HWR#*** and ***HRD#*** cycles are faster than the **ZR36710** timing allows, then ***HACK#*** is used as a dynamic wait-state request, holding off the completion of the ***HWR#*** or ***HRD#*** cycle until the **ZR36710** has time to latch data to/from the data bus. A fast host that follows the VMI 1.4 specifications may connect ***HACK#*** to the signal named READY in the VMI 1.4 specs.

TABLE 8. Type B Transfers

Direction	Sequence of Type B Handshakes
Write	1. Host asserts ***HCS#*** and selects an address on ***HA[3:0]***. 2. Host places data on ***HD*** lines and asserts ***HWR#***. 3. **ZR36710** asserts ***HACK#*** upon sampling ***HWR#*** low. 4. **ZR36710** latches-in the data on the ***HD*** lines and de-asserts ***HACK#***. 5. Host de-asserts ***HWR#*** and ceases to drive the ***HD*** lines. Note: The host may ignore ***HACK#*** providing that ***HWR#*** meets minimum timing requirements.
Read	1. Host asserts ***HCS#*** and selects an address on ***HA[3:0]***. 2. Host asserts ***HRD#***, indicating to the **ZR36710** that it requests data. 3. **ZR36710** asserts ***HACK#*** upon sampling ***HRD#*** low. 4. **ZR36710** places the data on the ***HD*** lines and de-asserts ***HACK#***. 5. Host latches-in the data on the ***HD*** lines and de-asserts ***HRD#***. 6. **ZR36710** ceases to drive the ***HD*** lines upon sampling ***HRD#*** high. Note: The host may ignore ***HACK#*** providing that ***HRD#*** meets minimum timing requirements.

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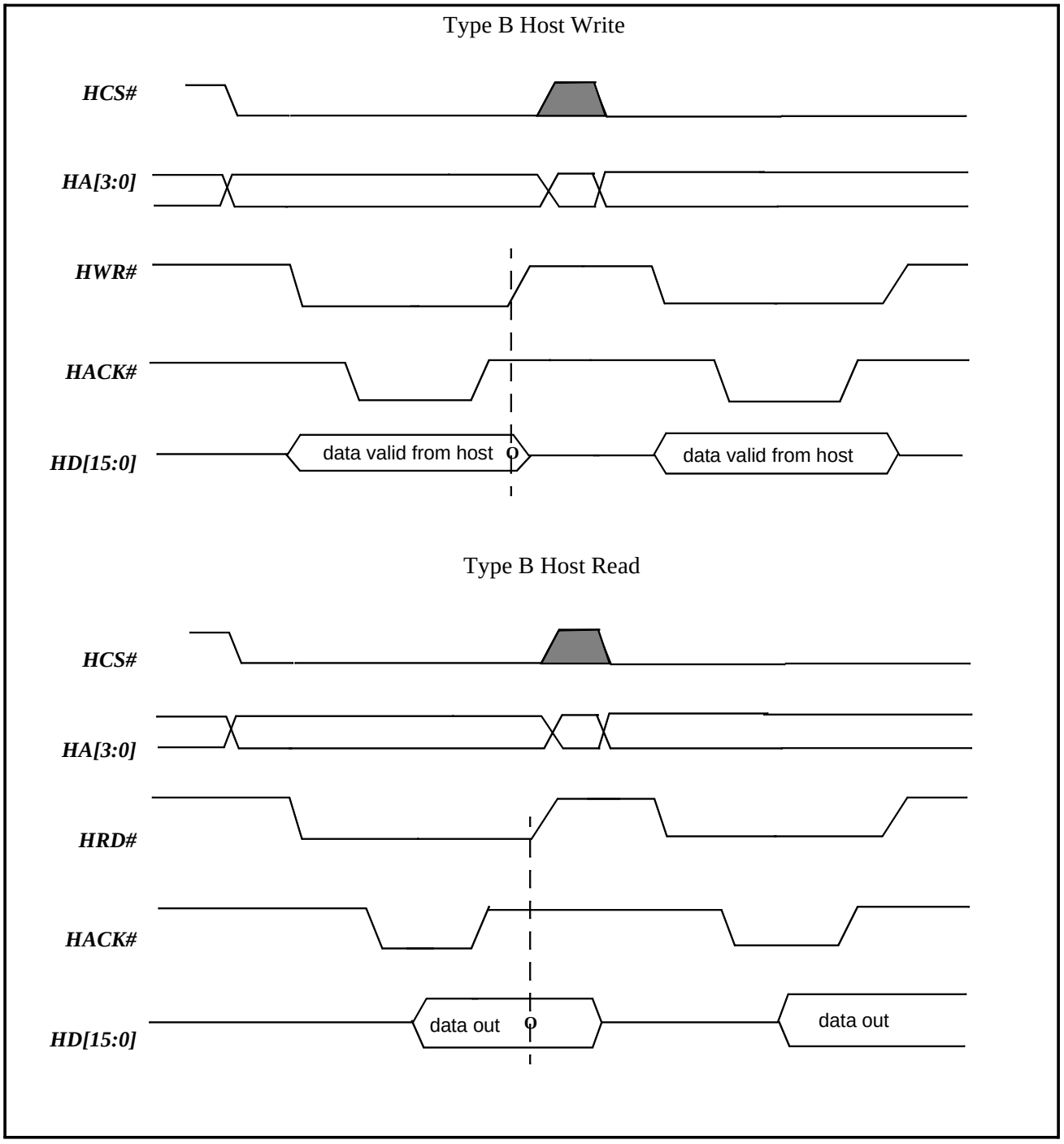

FIGURE 14. Host interface protocol -Type B. ***HD[15:0]*** can also be ***HD[7:0]*** for 8-bit interface.

4.3.3 Address/Register Space and Register Access

Table 9 provides a map of the **ZR36710** host registers. The 4-bit address bus (***HA[3:0]***) of the **ZR36710** allows for 16 addressable, 16-bit register locations.

TABLE 9. ZR36710 Host Address Space

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

Complete 16-bit Transfers Per Register Access

Each write to/read from a **ZR36710** register must be a complete 16-bit transfer. When the host data bus is only 8-bits, every write to/read from a **ZR36710** register must consist of two consecutive byte-accesses to the same address, m.s. byte first. After writing/reading the m.s byte to/from a particular register, the host must not write to/read from a different address until having written/read the l.s. byte first. The only exception to this rule regards the Coded Bitstream Register as described below.

Complete Accesses for Each Register

Each register must be completely accessed prior to accessing a different register. For example, if a parameter requires that 16 words must be written to the Parameter Data Register, then all 16 words must be written consecutively prior to access to a different register. The only exception to this rule regards the Coded Bitstream Register which is explained below.

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Exception: Coded Bitstream Register

In 16-bit mode, code-writes to the Coded Bitstream Register can be done in the middle of transferring other types of data. For example, if a parameter that consists of 16 words is written to the Parameter Data Register, one or more code words can be written to the Coded Bitstream Register after writing any partial number of the parameter words. Once access to the Coded Bitstream Register is complete, then access to the previously-accessed register must resume.

In 8-bit mode, code-writes to the Coded Bitstream Register do not have to be complete 16-bit writes. Odd-numbered byte transfers (including just a single byte) are allowed. Also, as with 16-bit transfers, code-writes to the Coded Bitstream Register can be done in the middle of transferring other types of data, but for 8-bit transfers the transfers do not need to be word-aligned.

4.3.4 Interrupt Signal - *HIRQ#*

The **ZR36710** has a single interrupt request output, ***HIRQ#***. This active-low signal is triggered upon one or more events that occur within the device. Two host registers, the Interrupt Mask Register (IMR) and Interrupt Status Register (ISR) reflect which event triggered the interrupt and allows selection of which events can trigger an interrupt and which events cannot. ***HIRQ#*** remains asserted until the host reads the ISR.

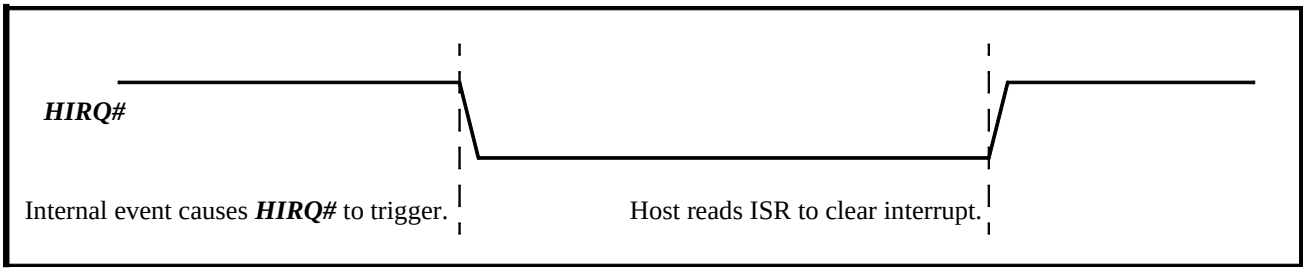

FIGURE 15. ***HIRQ#*** behavior

Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” explains the IMR and ISR, including which events are available to trigger interrupts.

4.3.5 Coded Data Request for Host Bus Code Transfers - *HRDY*

When the source of the coded bitstream is the host interface (*CodeSource*[1] = 1), the host writes the bitstream to the Coded Bitstream Register of the **ZR36710**.

The ***HRDY*** output pin indicates to the host if the **ZR36710** can be accessed with coded bitstream. A high level on ***HRDY*** is interpreted by the host as follows: up to *CodBurstLen*[1] (valid values are 4, 8, 16, 32 or 64) code bytes can be written without having to check ***HRDY*** again. After ***HRDY*** is de-asserted, a

1. *CodeSource* and *CodeBurstLen* are bits of the *SysConfig* set-up parameter. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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number of code bytes may be further written to the **ZR36710**, such that the total number of bytes, written since the last time ***HRDY*** was high, will be *CodBurstLen*[1].

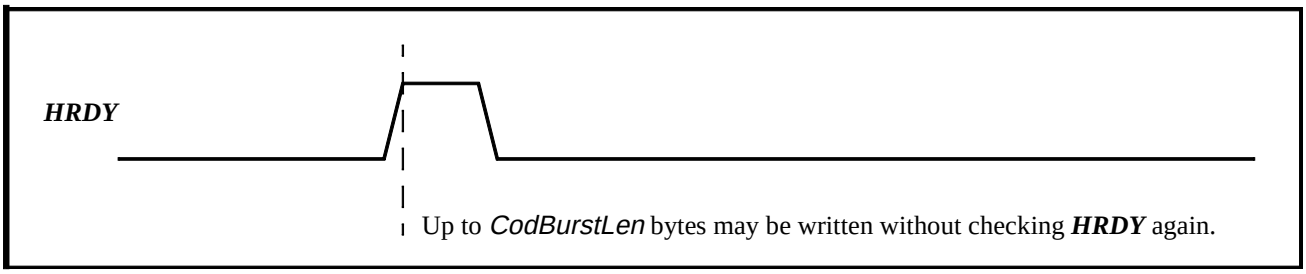

FIGURE 16. ***HRDY*** behavior

HRDY operates the same way in both Type A and Type B protocols. Its level is also represented by the **HRDY** bit in the **STATUS1**[2] register. It has a delay of 6 ***PCLK***s (74ns @ 81.0MHz) from the status change in the buffer to the level change at the output pin. ***HRDY*** has no functionality for accesses to other registers than the Coded Bitstream Register nor if the DVD-DSP (or CD-DSP) interface provides the coded data. If the bitstream is provided via the DVD-DSP or CD-DSP interfaces, ***HRDY*** will toggle depending on the amount of data transferred to the device, but the signal does not need to be monitored.

Data is internally transferred from the Coded Bitstream Register to a code FIFO. If the host does not monitor the ***HRDY*** pin or **HRDY** status bit then the host risks overwriting unused data within the FIFO, causing bitstream errors.

Alternative: Using *HACK#* instead of *HRDY* in Type B Transfers to the Coded Bitstream Register

In some system designs that use the Coded Bitstream Register, polling the ***HRDY*** pin or **HRDY** status bit may be inefficient and not a viable option. In this case, ***HACK#*** is used to indicate when data can be written to the coded bitstream register. This option is only available for Type B transfers and is enabled by setting the *HACKMode* bit of the *SysConfig*[1] set-up parameter to 1.

For writes to the Coded Bitstream Register, ***HACK#*** operates as shown in Figure 14 while ***HRDY*** is high. If ***HRDY*** is low, ***HACK#*** will remain asserted until ***HRDY*** toggles high. The host should not complete its write cycle (de-activate ***HWR#***) until ***HACK#*** is de-activated.

1. *CodBurstLen* and *HACKMode* are bits of the *SysConfig* set-up parameter. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.
2. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

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4.3.6 General Purpose Signals - *GPAI/O[1:0]*, *GPSI* and *GPSO*

The **ZR36710** has 4 general purpose signals. Two signals are available to the host as general purpose inputs and outputs programmable through the ADP while the remaining two are allocated as one input and one output available only to the DVP:

- ***GPAI/O[0]*** and ***GPAI/O[1]***: programmable through the ADP.
- ***GPSI*** and ***GPSO***: are an input and an output, respectively, of the DVP.

The SETIO[1] ADP command determines the direction (either input or output) for each of the ***GPAI/O[1:0]*** pins, allows setting the level (high or low) on the pin(s) designated as output(s) and returns to the host the status level (high or low) on pin(s) designated as input(s).

If one or both of the ***GPAI/O[1:0]*** pins is designated as an output, then when the status of the pin(s) is returned to the host, this level reflects the output status.

4.4 DVD-DSP and CD-DSP Interfaces

The **ZR36710** has two input ports for interfacing to a DVD-DSP and/or CD-DSP device.

- A DVD-DSP parallel port for receiving coded data from a DVD-DSP device.
- A CD-DSP I^2S serial port, for receiving CD disc data from a CD-DSP device (or a DVD-DSP that emulates a CD-DSP).

The pins of the serial port are shared with ***HD[14:12]***. If the **ZR36710** is configured to receive data from its DVD-DSP interface and also is configured for an 8-bit host data bus, ***HD[14:12]*** are then automatically defined as the CD-DSP serial port.

1. See Section 12.4 “Set-up Commands” for an explanation on configuring ***GPAIO[1:0]*** pins via ADP commands.

4.4.1 DVD-DSP Parallel Data Interface

The DVD-DSP interface is an 8-bit data port with a programmable synchronous or asynchronous 4-signal control bus. This interface is compatible with several DVD-ROM controller chipsets. Supported disc sectors include DVD, VideoCD, CD-I (FMV) or CD-DA.

TABLE 10. DVD-DSP to **ZR36710** Handshake

Sequence of DVD-DSP Handshakes
1. **ZR36710** asserts ***DVDREQ***.
2. DVD-DSP device places data on ***DVDDAT[7:0]*** lines.
3. DVD-DSP device asserts ***DVDSOS*** if the data coincides with the start of a sector.
4. DVD-DSP device asserts ***DVDVALID*** to indicate that the ***DVDDAT[7:0]*** and ***DVDSOS*** lines contain valid information.
5. DVD-DSP device asserts ***DVDSTRB*** to latch these signals into the **ZR36710** on the effective edge of ***DVDSTRB***.
6. While ***DVDREQ*** is asserted, steps 2 through 6 are repeated for continuous data transfer. Depending on the operation of the DVD-DSP device, ***DVDVALID*** may be remain asserted during multiple transfers of data.
7. **ZR36710** de-asserts ***DVDREQ*** with only 8 bytes of room left in the **ZR36710**'s internal code FIFO.
8. DVD-DSP device transfers up to 6 bytes as described in steps 2 through 6 to complete the transfer.
The cycle repeats when ***DVDREQ*** is re-asserted.
Restriction 1: *CodeSource*[a] = 0, *IFMode*[a] = 0, *DVDReqEnable*[a] = 0 and *CodBurstLen*[a] = 16, 32 or 64.
Restriction 2: The minimum cycle of ***DVDSTRB*** is 45ns (allowing for data clocks of up to 21 MHz).
Note 1: ***DVDREQ*** is asserted when there is room for *CodBurstLen* bytes in the **ZR36710** internal code FIFO. The host has the option of disabling ***DVDREQ*** by setting *DVDReqEnable* = 1.
Note 2: If ***DVDVALID*** is inactive when ***DVDSTRB*** is asserted, the information on all input signals is ignored.
Note 3: The above described behavior is for asynchronous operation (*DVDREQSync*[a] = 0) See below for details.

a. *CodeSource* and *CodBurstLen* are bits of the *SysConfig* set-up parameter. *IFMode* and *DVDREQSync* are bits of the *SDConfig* set-up parameter. *DVDReqEnable* is a bit of the *PlaybackMode* set-up parameter. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

Some DVD-DSP devices generate a continuous clock for ***DVDSTRB*** and will qualify which pulses contain valid data with the ***DVDVALID*** signal. In turn, some of these devices expect that the ***DVDREQ*** signal from the **ZR36710** is synchronized to this continuous clock. The *DVDREQSync* bit of the *SDConfig*[1] set-up parameter, shown in Table 11 , selects whether or not the **ZR36710** must generate ***DVDREQ*** synchronized to ***DVDSTRB***.

1. See Section 5.1 "General Set-up Parameters and Microcode - Reg. 0x0 and 0x1" for an explanation on loading set-up parameters to the **ZR36710**.

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The active polarity of the control signals is programmable through various bits of the *SDConfig*[1] set-up parameter.

TABLE 11. Setting the active polarity of the DVD-DSP signals via the *SDConfig* set-up parameter

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.
Reserved bits must be 0.													
DVDREQSync	0 = DVDREQ operates asynchronously with DVDSTRB. Must be 0 if not applicable. 1 = DVDREQ is synchronized to DVDSTRB.												
REQPol	0 = ***DVDREQ*** is active-low. Must be 0 if not applicable. 1 = ***DVDREQ*** is active-high.												
VALIDPol	0 = ***DVDVALID*** is active-low. Must be 0 if not applicable. 1 = ***DVDVALID*** is active-high.												
SOSPol	0 = ***DVDSOS*** is active-low. Must be 0 if not applicable. 1 = ***DVDSOS*** is active-high.												
STRBPol	0 = DVD-DSP signals are sampled on falling edge of ***DVDSTRB***. Must be 0 if not applicable. 1 = DVD-DSP signals are sampled on rising edge of ***DVDSTRB***.												

Figure 17 depicts an example of a handshaking protocol between the **ZR36710** and a DVD-DSP device. Detailed timing is given in Section 11. “DC and AC Characteristics”.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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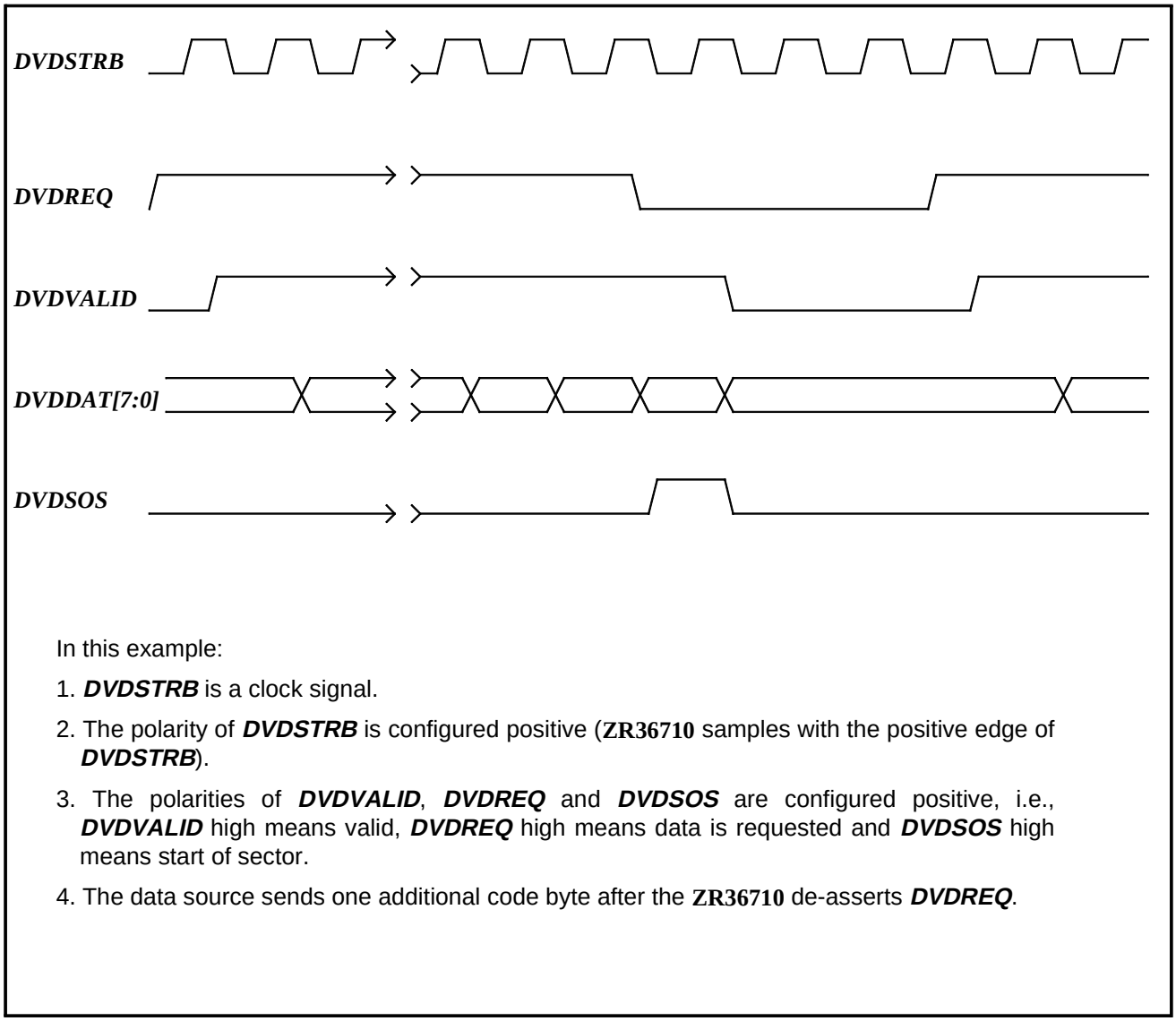

In this example:

1. ***DVDSTRB*** is a clock signal.
2. The polarity of ***DVDSTRB*** is configured positive (**ZR36710** samples with the positive edge of ***DVDSTRB***).
3. The polarities of ***DVDVALID***, ***DVDREQ*** and ***DVDSOS*** are configured positive, i.e., ***DVDVALID*** high means valid, ***DVDREQ*** high means data is requested and ***DVDSOS*** high means start of sector.
4. The data source sends one additional code byte after the **ZR36710** de-asserts ***DVDREQ***.

FIGURE 17. DVD-DSP Parallel Port (Handshaking Example)

4.4.2 CD-DSP Serial Data Interface

The CD-DSP interface is a 3-signal serial I^2S port. This interface is compatible with several CD-ROM controller chipsets and also with DVD-ROM controller chipsets that emulate this bus. Supported disc sectors include VideoCD, CD-I (FMV) or CD-DA (no DVD support).

The three signals that make up the CD-DSP interface are ***CDFRM***, ***CDDAT*** and ***CDCLK***. The following sub-sections explain each of these signals in detail.

4.4.2.1 *CDFRM* Signal

CDFRM is a frame synchronization input to the **ZR36710** that helps identify the start of each 16-bit data word transferred on the ***CDDAT*** line. ***CDFRM*** changes its level every 16, 24 or 32 ***CDCLK*** cycles as selected by the *CDPeriod* bits in the *SDConfig*[1] set-up parameter.

A ***CDFRM*** period consists of a complete ***CDFRM*** transition cycle (from rising edge to rising edge) so the period length is either 32, 48 or 64 ***CDCLK*** cycles.

For CD-DA data, DVP microcode determines which polarity of ***CDFRM*** indicates the left and right channels. For left channel audio to be presented while ***CDFRM*** is low, one version of microcode is required. For right channel audio to be presented while ***CDFRM*** is low, a different microcode is required. Refer to microcode release notes for further details.

TABLE 12. Configuring ***CDFRM*** via the *SDConfig* set-up parameter

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.
Reserved bits must be 0.													
CDPeriod			00b = ***CDFRM*** period is 32 ***CDCLK*** cycles. Must be 00b if not applicable. 01b = ***CDFRM*** period is 48 ***CDCLK*** cycles. 10b = ***CDFRM*** period is 64 ***CDCLK*** cycles. 11b = Reserved, do not use.										

4.4.2.2 *CDDAT* Signal

CDDAT is the data line in which data is organized in 16-bit words. Each word is aligned between two transitions (during the time ***CDFRM*** is either high or low without changing state) of the ***CDFRM*** signal. For both VideoCD and CD-DA data, DVP microcode determine both the bit and byte order. For example, a version of DVP microcode may determine that for VideoCD data, the **ZR36710** is expecting the data l.s. byte first and for each of the two bytes m.s. bit first and for CD-DA data, the **ZR36710** is expecting the data m.s. byte first and for each of the two bytes m.s. bit first. If the data is presented to the **ZR36710** in the wrong bit order, then the *CDBitSwap* bit of the *SDConfig* set-up parameter can be set to swap the bit order as shown in Table 13 . Bit-swapping from l.s. significant to m.s. significant is done on the entire 16-bit word and not for each individual byte, effectively performing byte-swapping as well.

The 16 bits are either left-justified (immediately after the transition of the ***CDFRM*** signal), one ***CDCLK*** cycle after the transition of the ***CDFRM*** signal, or right-justified, as specified by the *CDJust* bits in the *SDConfig* set-up parameter.

Note that if the first bit appears one ***CDCLK*** cycle after the transition of the ***CDFRM*** signal and the period of the ***CDFRM*** signal is 32 ***CDCLK*** cycles, the last bit of the word will appear after the next transition of the ***CDFRM*** signal.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters and microcode to the **ZR36710**.

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TABLE 13. Configuring ***CDDAT*** via the *SDConfig* set-up parameter

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.
Reserved bits must be 0.													
CDJust			00b = ***CDDAT*** data is left-justified. Must be 00b if not applicable. 01b = ***CDDAT*** data is left-justified with one ***CDCLK*** cycle delay. 10b = ***CDDAT*** data is right-justified. 11b = Reserved, do not use.										
CDBitSwap			0 = No bit swapping on CD-DSP interface. Must be 0 if not applicable. 1 = Bit swapping (reverse order l.s. to m.s.) per word on CD-DSP interface.										

4.4.2.3 *CDCLK* Signal

CDCLK is the clock signal used to latch the ***CDDAT*** and ***CDFRM*** signals into the **ZR36710**. The edge (rising or falling) that is used to latch these signals is specified by the *CDEdge* bit in the *SDConfig*[1] set-up parameter.

TABLE 14. Configuring ***CDCLK*** via the *SDConfig* set-up parameter

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.
Reserved bits must be 0.													
CDEdge			0 = CD-DSP interface signals are sampled on falling edge of ***CDCLK***. Must be 0 if not applicable. 1 = CD-DSP interface signals are sampled on rising edge of ***CDCLK***.										

4.4.2.4 Timing and Restrictions

Table 15 lists the restrictions for a system that uses the CD-DSP interface.

TABLE 15. CD-DSP Restrictions

Restrictions for CD-DSP Interface
Restriction 1: *CodeSource*[a] = 0, *IFMode*[a] = 1 and *MajorType*[a] = 1.
Restriction 2: ***HWID*** = **GND**.
Restriction 3: This interface supports up to 8x CD drives. Because the **ZR36710** may have to perform block decoding and handle other tasks, the actual supported drive speed may be less. This is explained in greater detail in a separate application note regarding VideoCD playback via this interface.

a. *CodeSource* is a bit of the *SysConfig* set-up parameter. *IFMode* is a bit of the *SDConfig* set-up parameter. *MajorType* is a bit of the *DiscType* set-up parameter. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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Figure 18 and Figure 19 show examples of various CD-DSP interface configurations. Both figures give examples of transfers that are m.s. bit first with no byte swapping. Detailed timing is given in Section 11. “DC and AC Characteristics”.

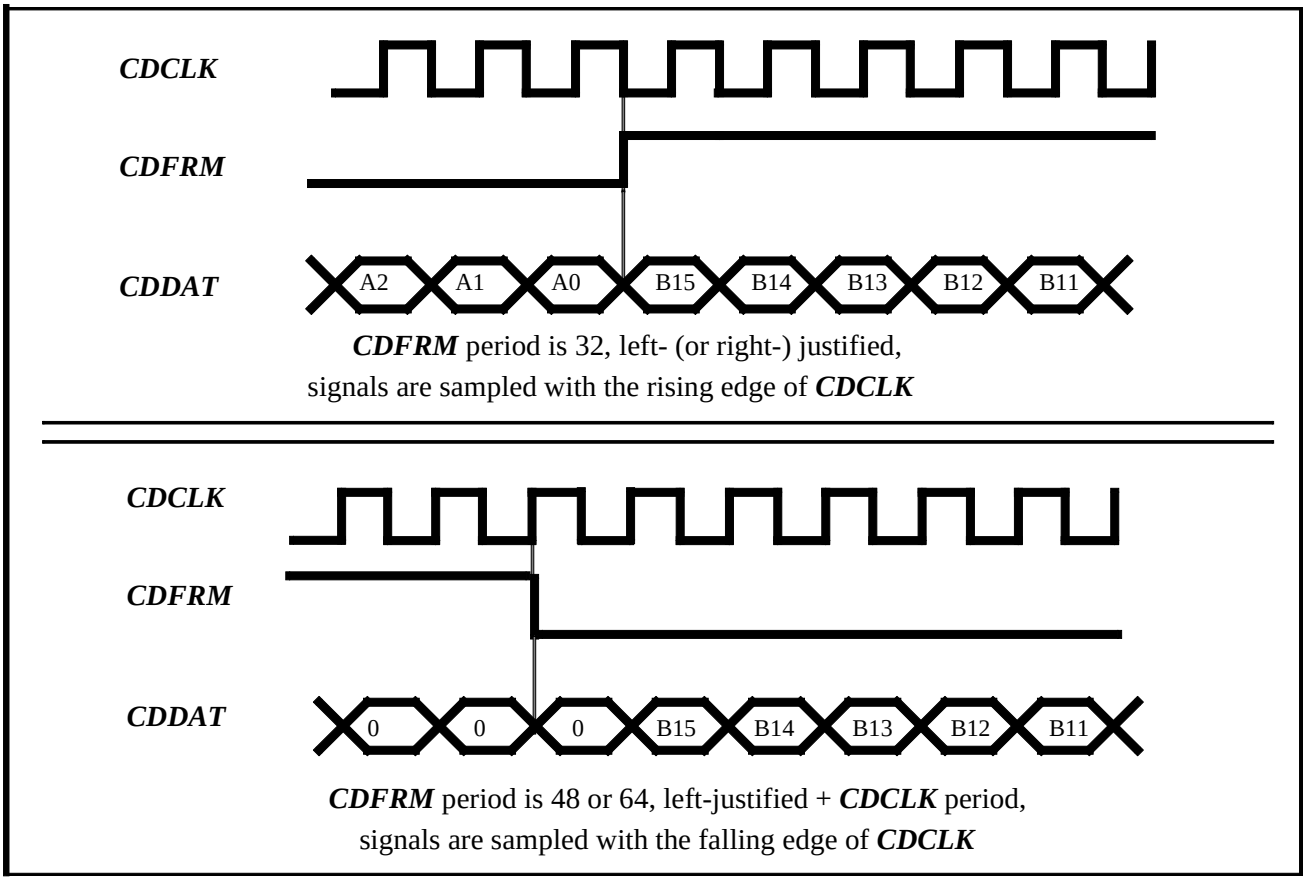

FIGURE 18. CD-DSP interface signals when playing back CD type discs (Examples)

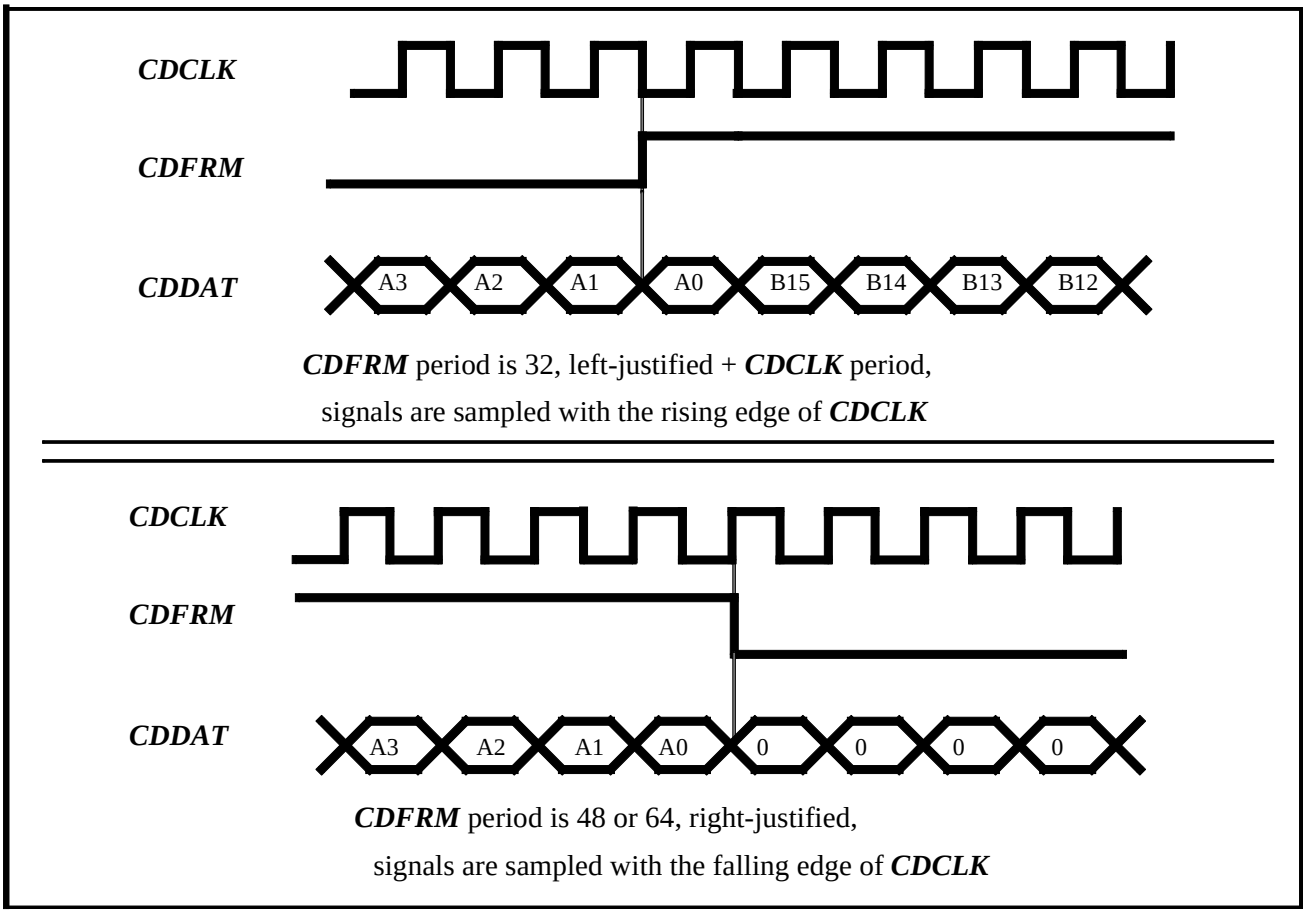

FIGURE 19. CD-DSP interface signals when playing back CD type discs (Examples, cont.)

4.5 Video Interface

The video interface of the **ZR36710** consists of a pixel bus (selectable 8-bit or 16-bit), a pixel bus tri-state pin, horizontal and vertical sync signals, a field-indication signal, a composite blank output, a pixel clock and a 2x pixel clock. The pixel bus provides either 16-bit pixels at 13.5 MHz (CCIR601-compatible) or 8-bit “half-pixels” at 27 MHz (CCIR656-compatible, including optional sync codes). The pixels are output in YUV 4:2:2 format. This interface allows direct pin-to-pin interconnection with several video encoders and with other Zoran devices: (e.g. ZR36125, ZR36067, ZR36060).

The **ZR36710** incorporates programmability for sync waveforms, field-indication and composite blank waveforms, active video regions, image regions, and programmable background colors to be displayed outside the active and image regions. The **ZR36710** can operate as either a sync master, generating the syncs, field indication and pixel clocks, or it can operate as a slave, receiving as inputs these same signals. This allows flexibility to condition the video output as required by the system design.

4.5.1 Overview of Master and Slave Modes

The **ZR36710** operates as either a sync master or a sync slave as indicated by the polarity of the ***VMASTER*** input pin. Figure 20 and Figure 21 show the mode of operation dictated by the ***VMASTER*** pin. This pin's level must remain constant throughout the operation of the **ZR36710**. It can only be changed during RESET.

4.5.1.1 Sync-Master Mode

In sync master mode, the **ZR36710** generates the video clocks, the horizontal and vertical sync signals and field-indication signal. The ***HSYNC***, ***VSYNC*** and ***FI*** outputs are locked to the internal timing of the device. Their waveform specifications are programmable as explained in Section 4.5.3 "Configuration of Syncs, Field Indication and Composite Blanking". Figure 20 illustrates the sync-master mode.

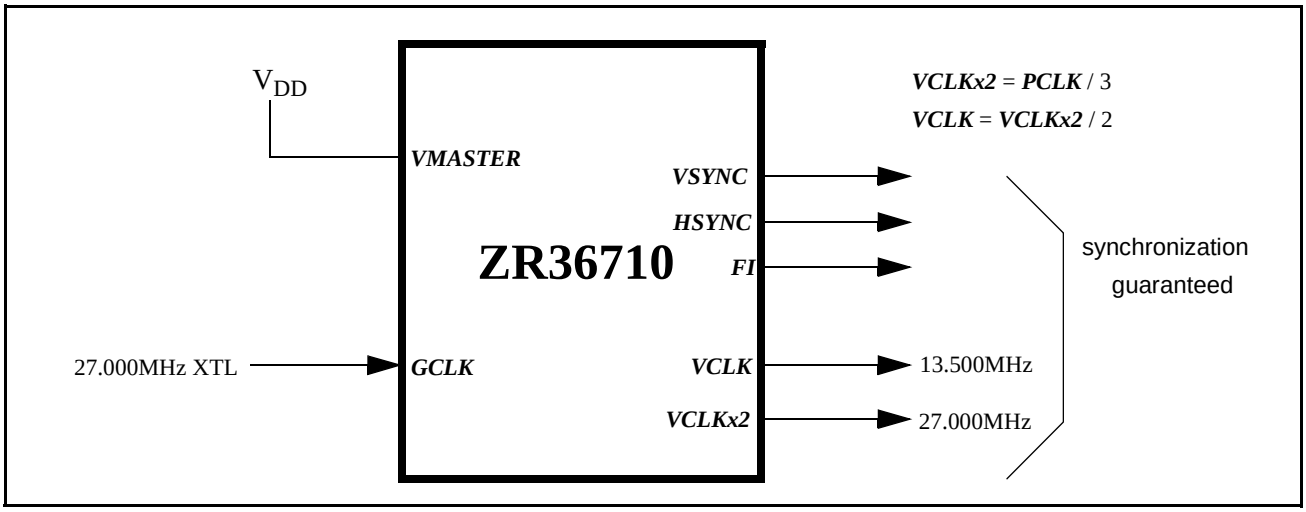

FIGURE 20. Video Sync Master-Mode

4.5.1.2 Sync-Slave Mode

In sync slave mode, the video clocks, horizontal and vertical syncs and field-indication (optional in slave mode) are inputs to the **ZR36710**. Figure 21 illustrates the sync-slave mode.

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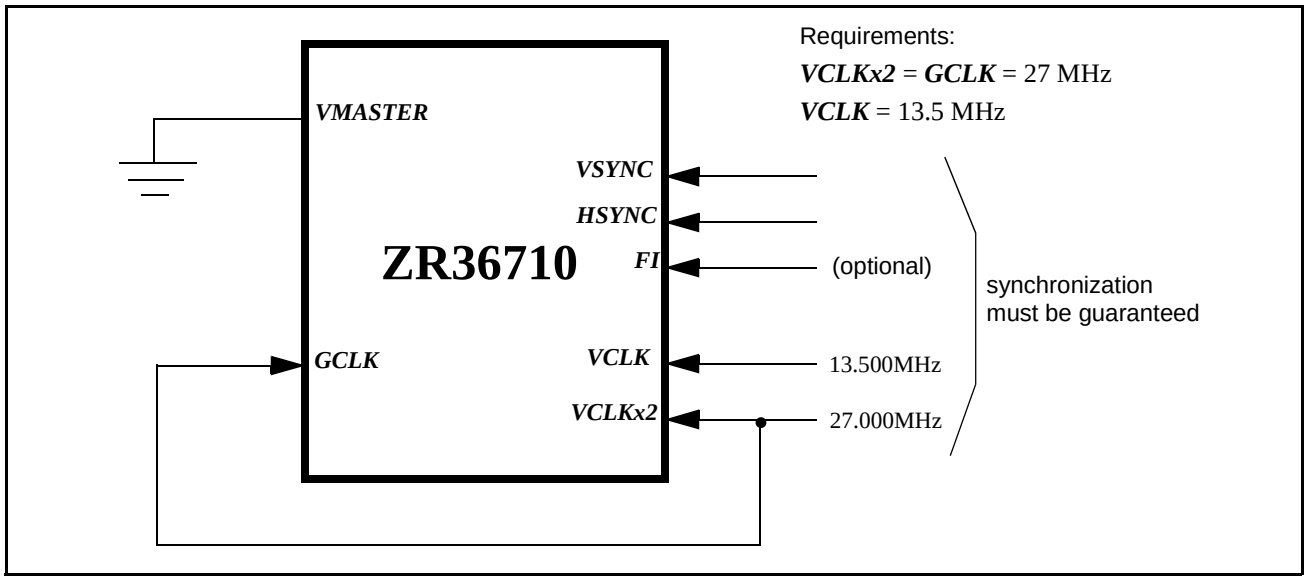

FIGURE 21. Video Sync Slave-Mode

4.5.2 Video Clocks

In master mode, the video clocks ***VCLK*** and ***VCLKx2*** indicate to the system when to properly sample the outputs (syncs, field indication, composite blank and pixel data) on the video interface. In slave mode, the video clocks indicate to the **ZR36710** when to properly sample the inputs (syncs and field indication) on the video interface and when to present the outputs (composite blank and pixel data) to the system. The video clocks are described in Table 16 .

TABLE 16. Video Clock Signals

Clock	Description
VCLKx2	2x pixel clock. In master mode, its rising edge is used to indicate to the system that the outputs on the video interface contain valid data. In slave mode, its rising edge is used to sample the syncs and (optional) field indication inputs and indicate to the system that the outputs on the pixel and composite blank pins contain valid data.
VCLK	Pixel clock. When operating in 16-bit pixel mode, it indicates which rising edge of ***VCLKx2*** is used as the data qualifier on the video interface. When operating in 8-bit pixel mode, it indicates which rising edge of ***VCLKx2*** is used as the sync, field indication and Y component qualifier. The *VCLKPol* bit in the *VidConfig*[a] set-up parameter indicates which polarity of ***VCLK*** qualifies the rising edge of ***VCLKx2*** as follows: *VCLKPol* = 0, The rising edge of ***VCLKx2*** while ***VCLK*** is low qualifies the data. *VCLKPol* = 1, The rising edge of ***VCLKx2*** while ***VCLK*** is high qualifies the data.

a. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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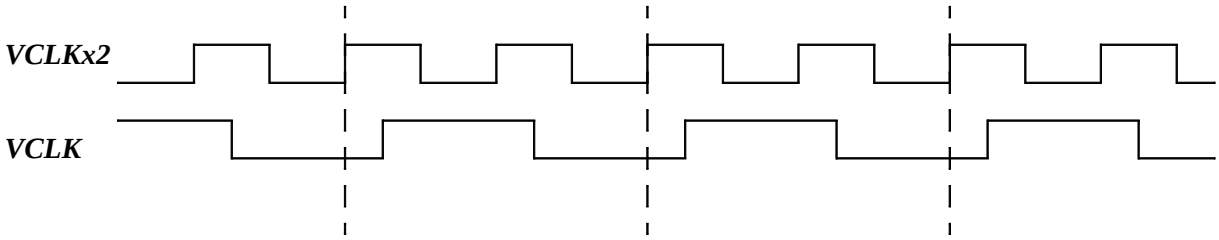
In Figure 22, syncs and field indication signals would be sampled by either the video encoder (master mode) or the **ZR36710** (slave mode) on the rising edge of ***VCLKx2*** while ***VCLK*** is low. The system would sample the pixel data (16-bit pixel bus) and composite blank signal at this time.

With an 8-bit pixel bus, pixel data is presented at the twice the pixel rate (half-pixels) and should be sampled by the system on every rising edge of ***VCLKx2***. As shown in Figure 22, the Y component is valid on the rising edge of ***VCLKx2*** when ***VCLK*** is low. One pixel is transmitted each ***VCLK*** period, whether the pixel bus is 8 bits or 16 bits.



Note: dashed lines indicate time at which signals on the video interface are valid (16-bit pixel mode).

FIGURE 22. Video interface data qualification every other rising edge of ***VCLKx2*** (*VCLKPol* = 0).

4.5.3 Configuration of Syncs, Field Indication and Composite Blanking

In master mode, the **ZR36710** requires the host to load various set-up parameter values to properly generate the ***HSYNC***, ***VSYNC***, ***FI*** and ***CBLANK*** waveforms. In slave mode, different values for these set-up parameters are required to allow the device to properly process the ***HSYNC***, ***VSYNC*** and (optional) ***FI*** inputs in order to output the desired ***CBLANK*** waveform and present pixel data at the desired time. The following sub-sections explain the set-up parameter options for both master and slave modes.

4.5.3.1 Sync Parameters - Master Mode

Table 17 shows which set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) configure the waveforms of the ***HSYNC***, ***VSYNC*** and ***FI*** outputs when the **ZR36710** operates in master mode. The ***CBLANK*** configuration is the same for both master and slave modes so its configuration is explained separately in Section 4.5.3.3 “CBLANK Generation in Master and Slave Modes”.

TABLE 17. ***HSYNC***, ***VSYNC*** and ***FI*** Configuration in Master Mode

Signal	Parameters that define waveform in sync master mode
HSYNC	*Htotal*: Total number of pixels per line = number of ***VCLK***s between leading edges of consecutive ***HSYNC*** pulses. *Htotal* must be an even number. Maximum value is 1022. Typical NTSC and PAL values are: *Htotal* = 858 (NTSC). *Htotal* = 864 (PAL).
	HSyncSize: Width of ***HSYNC*** active pulse measured in number of pixels (***VCLK***s). Minimum value is 8. Maximum value is (*Htotal*/2 - 1).
	HSPol: Polarity of ***HSYNC*** signal during the active pulse. *HSPol* is a bit of the *VidConfig* set-up parameter. The allowed values are shown below.
	HEdge: Transition edge of ***HSYNC*** after which the first ***VCLK*** indicates pixel #0 (the first pixel) of that line. This edge is called the "effective" edge of ***HSYNC***. *HEdge* is a bit of the *VidConfig* set-up parameter. *HEdge* should be selected so that the leading edge is the effective edge: *HSPol* = 0, *HEdge* = 0: Leading (falling) edge of active-low ***HSYNC*** indicates the first pixel in a line. *HSPol* = 1, *HEdge* = 1: Leading (rising) edge of active-high ***HSYNC*** indicates the first pixel in a line.
VSYNC	*Vtotal*: Total number of lines per display frame = number of ***HSYNC*** pulses between every other ***VSYNC*** pulse. Maximum value is 1023. Each display frame consists of two fields, Field I and Field II, whose size (in lines) is *Vtotal* / 2. Typical NTSC and PAL values are: *Vtotal* = 525 (NTSC). *Vtotal* = 625 (PAL).
	VSyncSize: Width of ***VSYNC*** active pulse measured in number of lines (***HSYNC***s). Minimum value is 1. Maximum value is (*Vtotal*/2 - 1).
	VSPol: Polarity of the ***VSYNC*** signal during the blanking region. *VSPol* is a bit of the *VidConfig* set-up parameter. The polarity of *VSPol* is defined as: *VSPol* = 0, Active-low blanking region. *VSPol* = 1, Active-high blanking region.
	VEdge: Transition edge of ***VSYNC*** after which the first ***HSYNC*** pulse indicates line #0 (the first line) of that field. This edge is called the "effective" edge of ***VSYNC***. *VEdge* is a bit of the *VidConfig* set-up parameter and indicates the effective edge as follows: *VEdge* = 0, falling edge of ***VSYNC*** indicates the first line of a field. *VEdge* = 1, rising edge of ***VSYNC*** indicates the first line of a field.

TABLE 17. ***HSYNC***, ***VSYNC*** and ***FI*** Configuration in Master Mode

Signal	Parameters that define waveform in sync master mode
FI	*FIPol*: Defines the polarity of ***FI*** during Field I and Field II. *FIPol* is a bit of the *VidConfig* set-up parameter. *FIPol* = 0, ***FI*** is low during Field I and high during Field II. *FIPol* = 1, ***FI*** is high during Field I and low during Field II.
	FIVEdge: Selects which edge (leading or trailing) of ***VSYNC*** that ***FI*** toggles. *FIVEdge* is a bit of the *VidConfig* set-up parameter. *FIVEdge* = 0, ***FI*** transition precedes the leading edge of ***VSYNC*** by two pixels (see Figure 25). *FIVEdge* = 1, ***FI*** transition precedes the trailing edge of ***VSYNC*** by two pixels.
	FidSel: Selects which signal, either ***HSYNC*** or ***FI***, is used to indicate Fields I and II identification. *FidSel* is a bit of the *VidConfig* set-up parameter. If *Vtotal* is even, *FidSel* = 1 (***FI***). The allowed values are shown below.
	FidLevel: Indicates polarity of ***HSYNC*** or ***FI*** (determined by *FidSel*) during the effective edge of ***VSYNC*** that Fields I and II are determined. *FidLevel* is a bit of the *VidConfig* set-up parameter. *FidSel* = 0, *FidLevel* = 0: ***HSYNC*** sampled low on the effective edge of ***VSYNC*** determines Field I. ***HSYNC*** sampled high on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 0, *FidLevel* = 1: ***HSYNC*** sampled high on the effective edge of ***VSYNC*** determines Field I. ***HSYNC*** sampled low on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 1, *FidLevel* = 0: ***FI*** sampled low on the effective edge of ***VSYNC*** determines Field I. ***FI*** sampled high on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 1, *FidLevel* = 1: ***FI*** sampled high on the effective edge of ***VSYNC*** determines Field I. ***FI*** sampled low on the effective edge of ***VSYNC*** determines Field II.
Restrictions on *Htotal* and *Vtotal*: *Htotal* x *Vtotal* x frame rate (either 30/1.001 or 25) = ***VCLK***, ***VCLK*** = 13.5 MHz.	

Figure 23 gives an example of how these parameters are used to indicate the waveforms of both ***HSYNC*** and ***VSYNC***.

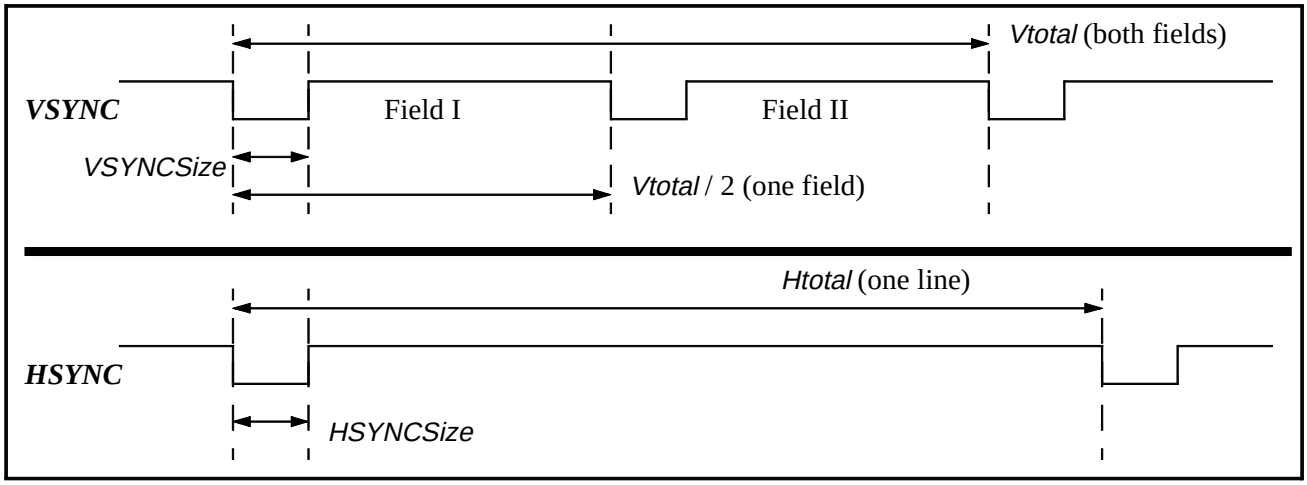


FIGURE 23. ***HSYNC*** and ***VSYNC*** with *HSPol* = *VSPol* = 0 (not to scale)

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Figure 24 shows the edge timing between ***HSYNC*** and ***VSYNC*** in master mode. The **ZR36710** guarantees that the leading edge of ***VSYNC*** will trail the leading edge of ***HSYNC*** by four pixels for Field I. For Field II, the leading edge of ***VSYNC*** trails the midpoint of line (int(*Vtotal* / 2) + 1) by four pixels. In this figure, it is assumed that both ***HSYNC*** and ***VSYNC*** are active-low, thus their leading edges are both falling edges.

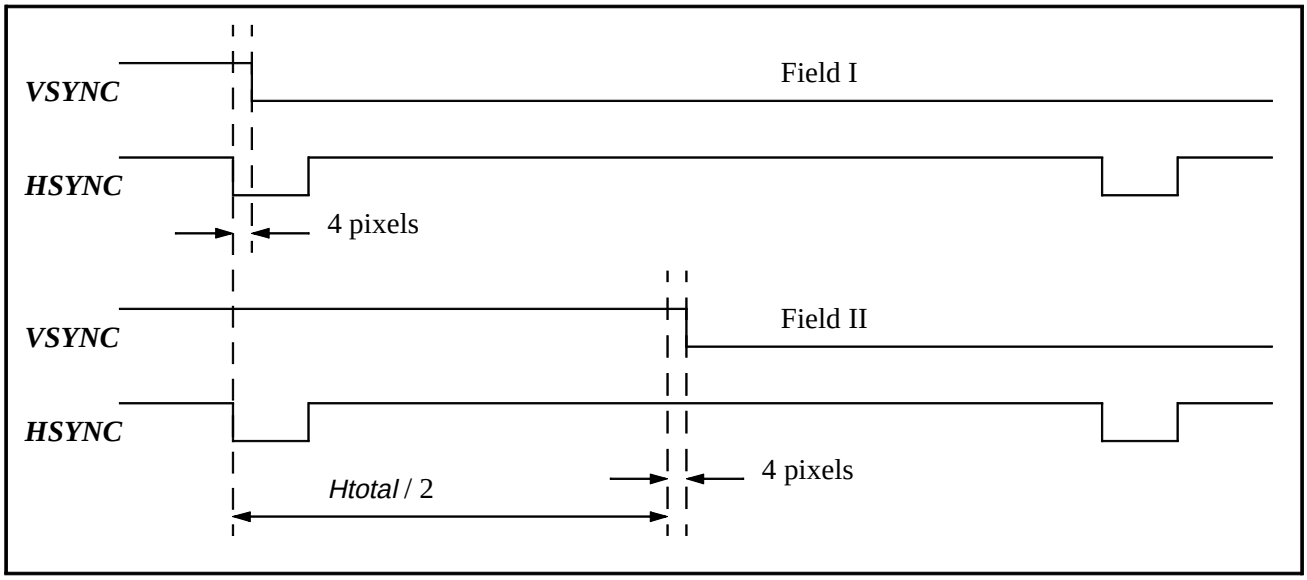

FIGURE 24. ***VSYNC*** always trails ***HSYNC*** by 4 pixels in master mode (not to scale).

Figure 25 gives an example of how these parameters are used to generate ***FI*** in master mode. *FIVEdge* and *FIPol* indicate that ***FI*** will toggle high for Field I two pixels prior to the leading edge of ***VSYNC***.

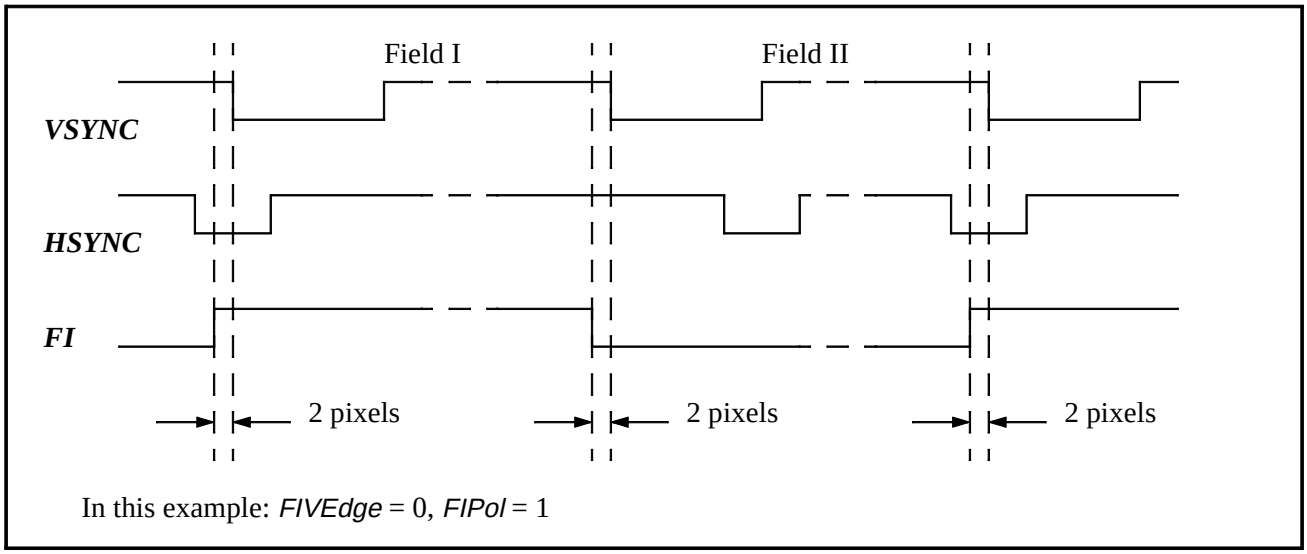

FIGURE 25. ***FI*** transition precedes leading edge of ***VSYNC*** by 2 pixels in master mode (not to scale).

4.5.3.2 Sync Parameters - Slave Mode

Table 18 shows which set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) allow the **ZR36710** to properly process the ***HSYNC***, ***VSYNC*** and (optional) ***FI*** inputs when the **ZR36710** operates in slave mode. The ***CBLANK*** configuration is the same for both slave and master modes so its configuration is explained separately in Section 4.5.3.3 “CBLANK Generation in Master and Slave Modes”.

TABLE 18. ***HSYNC***, ***VSYNC*** and ***FI*** Configuration in Slave Mode

Signal	Parameters that define waveform in sync slave mode
HSYNC	*Htotal*: Must be 0x0000.
	HSyncSize: Must be 0x0000.
	HSPol: Must be 0. *HSPol* is a bit of the *VidConfig* set-up parameter.
	HEdge: Transition edge of ***HSYNC*** after which the first ***VCLK*** indicates pixel #0 (the first pixel) of that line. This edge is called the “effective” edge of ***HSYNC***. *HEdge* is a bit of the *VidConfig* set-up parameter. *HEdge* should be selected so that the leading edge is the effective edge: *HEdge* = 0: Leading (falling) edge of active-low ***HSYNC*** indicates the first pixel in a line. *HEdge* = 1: Leading (rising) edge of active-high ***HSYNC*** indicates the first pixel in a line.
VSYNC	*Vtotal*: Must be 0x0000.
	VSyncSize: Must be 0x0000.
	VSPol: Must be 0. *VSPol* is a bit of the *VidConfig* set-up parameter.
	VEdge: Transition edge of ***VSYNC*** after which the first ***HSYNC*** pulse indicates line #0 (the first line) of that field. This edge is called the “effective” edge of ***VSYNC***. *VEdge* is a bit of the *VidConfig* set-up parameter and indicates the effective edge as follows: *VEdge* = 0, falling edge of ***VSYNC*** indicates the first line of a field. *VEdge* = 1, rising edge of ***VSYNC*** indicates the first line of a field.

TABLE 18. ***HSYNC***, ***VSYNC*** and ***FI*** Configuration in Slave Mode

Signal	Parameters that define waveform in sync slave mode
FI **(optional)**	*FIPol*: Must be 0. *FIPol* is a bit of the *VidConfig* set-up parameter.
	FIVEdge: Must be 0. *FIVEdge* is a bit of the *VidConfig* set-up parameter.
	FidSel: Selects which signal, either ***HSYNC*** or ***FI***, is used to indicate Fields I and II identification. *FidSel* is a bit of the *VidConfig* set-up parameter. If ***FI*** is not provided to the device, then *FidSel* = 0. If the number of lines per two fields is even, ***FI*** must be provided to the device and *FidSel* = 1. The allowed values are shown below.
	FidLevel: Indicates polarity of ***HSYNC*** or ***FI*** (determined by *FidSel*) during the effective edge of ***VSYNC*** that Fields I and II are determined. *FidLevel* is a bit of the *VidConfig* set-up parameter. *FidSel* = 0, *FidLevel* = 0: ***HSYNC*** sampled low on the effective edge of ***VSYNC*** determines Field I. ***HSYNC*** sampled high on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 0, *FidLevel* = 1: ***HSYNC*** sampled high on the effective edge of ***VSYNC*** determines Field I. ***HSYNC*** sampled low on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 1, *FidLevel* = 0: ***FI*** sampled low on the effective edge of ***VSYNC*** determines Field I. ***FI*** sampled high on the effective edge of ***VSYNC*** determines Field II. *FidSel* = 1, *FidLevel* = 1: ***FI*** sampled high on the effective edge of ***VSYNC*** determines Field I. ***FI*** sampled low on the effective edge of ***VSYNC*** determines Field II.

Figure 26 gives an example of how these parameters are used to identify Fields I and II in slave mode using the ***HSYNC*** and ***VSYNC*** inputs. In this case, the ***FI*** input is optional. Proper sampling of ***HSYNC*** with the effective edge of ***VSYNC*** requires that the effective edges of ***HSYNC*** and ***VSYNC*** do not fall within a 2-pixel window. Here, *HEdge* and *VEdge* indicate the effective edges of the input syncs and *FidSel* and *FidLevel* indicate the field determination.

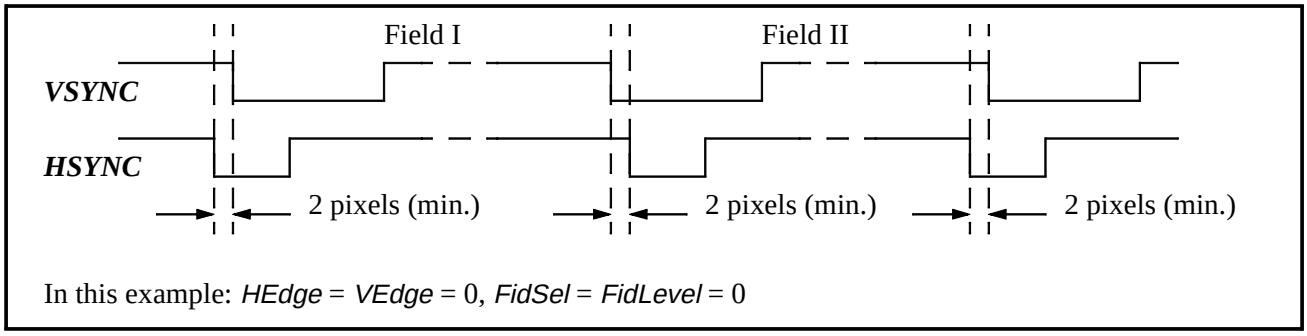

FIGURE 26. Field indication in slave mode using ***HSYNC*** and ***VSYNC*** (not to scale).

Figure 27 gives two examples of how these parameters are used to identify Fields I and II in slave mode using the ***FI*** and ***VSYNC*** inputs. Proper sampling of ***FI*** with the effective edge of ***VSYNC*** requires that the transition of ***FI*** and the effective edge of ***VSYNC*** do not fall within a 2-pixel window. Here, *VEdge* indicates the effective edge of ***VSYNC*** and *FidSel* and *FidLevel* indicate the field determination. Notice that a shift in ***FI*** by a minimum of four pixels (as shown here) can reverse the field determination. In any

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case, Field I and Field II are defined in Section 2.2 “Definitions” and the selection of the polarity of ***FI*** during the effective edge of ***VSYNC*** must match this definition.

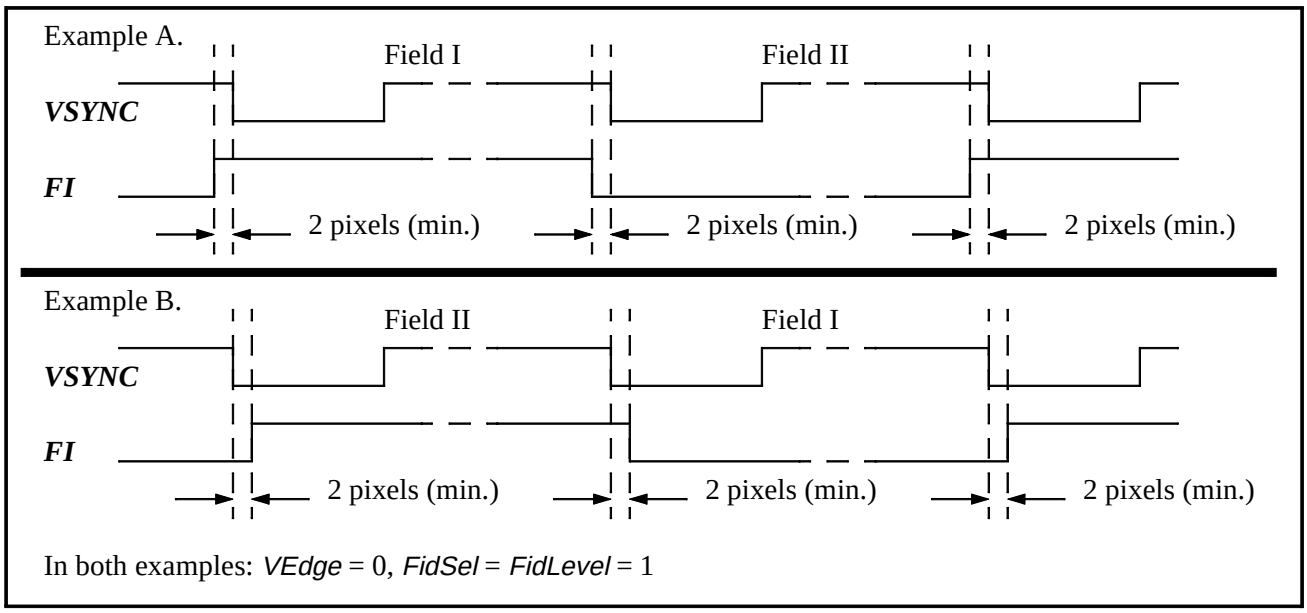

FIGURE 27. Field indication in slave mode using ***FI*** and ***VSYNC***. Must be at least 2 pixels between transition of ***FI*** and *VEdge* (not to scale).

4.5.3.3 *CBLANK* Generation in Master and Slave Modes

Table 19 shows which set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) configure the waveform of ***CBLANK***, the composite output. Figure 28 illustrates the waveform of ***CBLANK*** in relation to ***VSYNC***, ***HSYNC*** and these parameters.

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TABLE 19. ***CBLANK*** Configuration

Parameter	Description
CBPol	Defines the polarity of ***CBLANK***. *CBPol* is a bit of the *VidConfig* set-up parameter: *CBPol* = 0, ***CBLANK*** is active-low. *CBPol* = 1, ***CBLANK*** is active-high.
CBVStart	Number of lines (indicated by the number of ***HSYNC*** pulses) after the effective edge of ***VSYNC*** that ***CBLANK*** is inactive for Field I. For Field II, the *VSelect* bit of the *VidConfig* set-up parameter dictates the first line ***CBLANK*** is inactive from the effective edge of ***VSYNC***: *VSelect* = 1, ***CBLANK*** becomes inactive *CBVStart* ***HSYNC*** pulses after the effective edge of ***VSYNC*** for Field II. *VSelect* = 0, ***CBLANK*** becomes inactive (*CBVStart* + 1) ***HSYNC*** pulses after the effective edge of ***VSYNC*** for Field II.
CBVEnd	Number of lines (indicated by the number of ***HSYNC*** pulses) after the effective edge of ***VSYNC*** that ***CBLANK*** is inactive for Field I. For Field II, the *VSelect* bit of the *VidConfig* set-up parameter dictates the last line ***CBLANK*** is inactive from the effective edge ***VSYNC***: *VSelect* = 1, ***CBLANK*** becomes active *CBVEnd* ***HSYNC*** pulses after the effective edge of ***VSYNC*** for Field II. *VSelect* = 0, ***CBLANK*** becomes active (*CBVEnd* + 1) ***HSYNC*** pulses after the effective edge of ***VSYNC*** for Field II.
CBHStart	Number of pixels (indicated by the number of **VCLK** pulses) after the effective edge of ***HSYNC*** in which ***CBLANK*** becomes inactive.
CBHEnd	Number of pixels (indicated from the number of **VCLK** pulses) after the effective edge of ***HSYNC*** in which ***CBLANK*** becomes active.

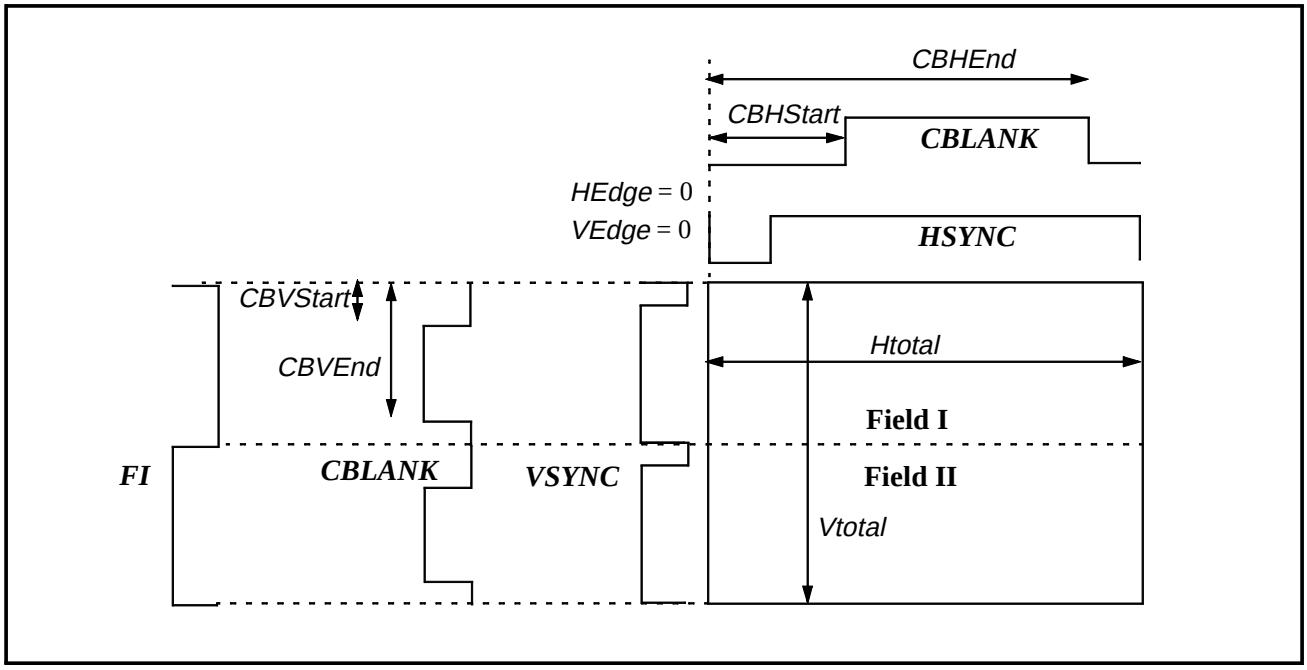

FIGURE 28. Illustration of ***CBLANK***.

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4.5.4 Definition of the Active Area, Image Area and Background Color

The “active” area within each field represents a window of the video region that decoded video, sub-pictures and OSD can be displayed. The size of this window is measured horizontally in pixels/line and vertically in lines/field. The position of this window is measured horizontally in pixels counted from the effective edge of ***HSYNC*** and vertically in lines counted from the effective edge of ***VSYNC***. Decoded video, sub-pictures and OSD cannot be displayed outside the defined active area. Table 20 lists the set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) that define the active video window within each field.

TABLE 20. Definition of Active and Image Areas

Region	Parameter	Parameters that define region
Active Area	*ActiveStartX*	Number of pixels (***VCLK***s) from the effective edge of ***HSYNC*** to the first active pixel (active pixel #0) of a line. *ActiveStartX* must be even.
	ActiveEndX	Number of pixels (***VCLK***s) from the effective edge of ***HSYNC*** to the last active pixel of a line, including this last pixel (active pixel #(*ActiveSizeX* - 1)). *ActiveEndX* must be even.
	ActiveSizeX	Horizontal size of active area (in pixels). Must be set to *ActiveEndX* - *ActiveStartX*.
	ActiveStartY	Number of lines (***HSYNC***s) from the effective edge of ***VSYNC*** to the start of the first active line of Field I (active line #0). The *VSelect* bit of the *VidConfig* set-up parameter determines how many lines after the first half-line of Field II the active region begins: *VSelect* = 1, the active region begins *ActiveStartY* lines. *VSelect* = 0, the active region begins (*ActiveStartY* + 1) lines.
	ActiveEndY	Number of lines (***HSYNC***s) from the effective edge of ***VSYNC*** to the end of the last active line of Field I. The *VSelect* bit of the *VidConfig* set-up parameter determines how many lines after the first half-line of Field II the active region ends: *VSelect* = 1, the active region ends *ActiveEndY* lines. *VSelect* = 0, the active region ends (*ActiveEndY* + 1) lines.
	ActiveSizeY	Vertical size (in lines) of active area in each field. Must be *ActiveEndY* - *ActiveStartY*.
Image Area	*ImageStartX*	Number of pixels (***VCLK***s) from the effective edge of ***HSYNC*** to the first image pixel of a line (image pixel #0). *ImageStartX* must be even.
	ImageEndX	Number of pixels (***VCLK***s) from the effective edge of ***HSYNC*** to the last image pixel of a line, including this last pixel (image pixel #(*ImageSizeX* - 1)). *ImageEndX* must be even.
	ImageSizeX	Horizontal size of image area (in pixels). Must be set to *ImageEndX* - *ImageStartX*.
	ImageStartY	Number of lines (***HSYNC***s) from the effective edge of ***VSYNC*** to the start of the first image line of Field I (image line #0). The *VSelect* bit of the *VidConfig* set-up parameter determines how many lines after the first half-line of Field II the image region begins: *VSelect* = 1, the image region begins *ImageStartY* lines. *VSelect* = 0, the image region begins (*ImageStartY* + 1) lines.
	ImageEndY	Number of lines from the effective edge of ***VSYNC*** to the end of the last image line of Field I. The *VSelect* bit of the *VidConfig* set-up parameter determines how many lines after the first half-line of Field II the image region ends: *VSelect* = 1, the image region ends *ImageEndY* lines. *VSelect* = 0, the image region ends (*ImageEndY* + 1) lines.
	ImageSizeY	Vertical size (in lines) of the image area in each field. Must be *ImageEndY* - *ImageStartY*.

The “image” area within each field represents a sub-window of active area. The image area can include the complete active area or a rectangle thereof. The size of this window is measured horizontally in pixels/line and vertically in lines/field. The position of this window is measured horizontally in pixels counted from the effective edge of ***HSYNC*** and vertically in lines counted from the effective edge of ***VSYNC***. Decoded video cannot be displayed outside the defined image area. As shown in Figure 29, the image area must either coincide with or fall completely within the active area. The primary purpose of having image area support is for display aspect ratio (e.g. Letterbox/Pan-scan) scaling as described in Section 7.4 “Defining the Image Area of the Scaled Image”. Table 20 lists the set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) that define the image area within each field

To properly determine which pixels and which lines define the active and image areas, the **ZR36710** has built-in pixel and line counters. The horizontal pixel counter is reset by an effective edge of ***HSYNC*** and pixels are counted on every other rising edge of ***VCLKx2***. The vertical line counter is reset by an effective edge of ***VSYNC*** and lines are counted on the effective edge of ***HSYNC***. If an effective edge of ***HSYNC*** occurs prior to counting *Htotal* pixels, the counter is still reset. The same can be said for *Vtotal* and the effective edge of ***VSYNC***.

For pixels that are outside the image area, pixel values are defined as the background color. The background color is defined by the set-up parameters (see Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1”) in Table 21 .

TABLE 21. Background color set-up parameters

ColorV **(0x08),** ***ColorY*** **(0x09),** ***ColorU*** **(0x0A)**	
ColorV	8-bit V component of the background color. The m.s. 8 bits must be 0x00.
ColorY	8-bit Y component of the background color. The m.s. 8 bits must be 0x00.
ColorU	8-bit U component of the background color. The m.s. 8 bits must be 0x00.

The background color on line 21 (closed caption) is forced to black (Y = 16, U = V = 128) no matter what the background color is defined as. Sub-picture and/or OSD data can be blended or overlaid anywhere within the active rectangle, including pixels that are out of the area occupied by the image itself. For data outside the image rectangle but within the active rectangle, the sub-picture and/or OSD data is overlaid on (or blended with) background pixels.

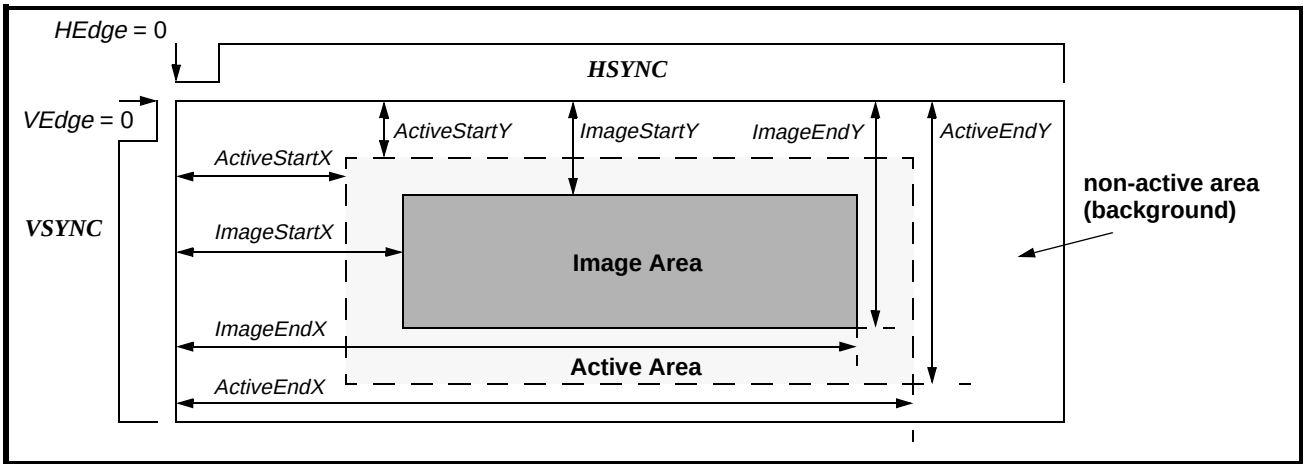

FIGURE 29. Definition of the “active” and “image” areas

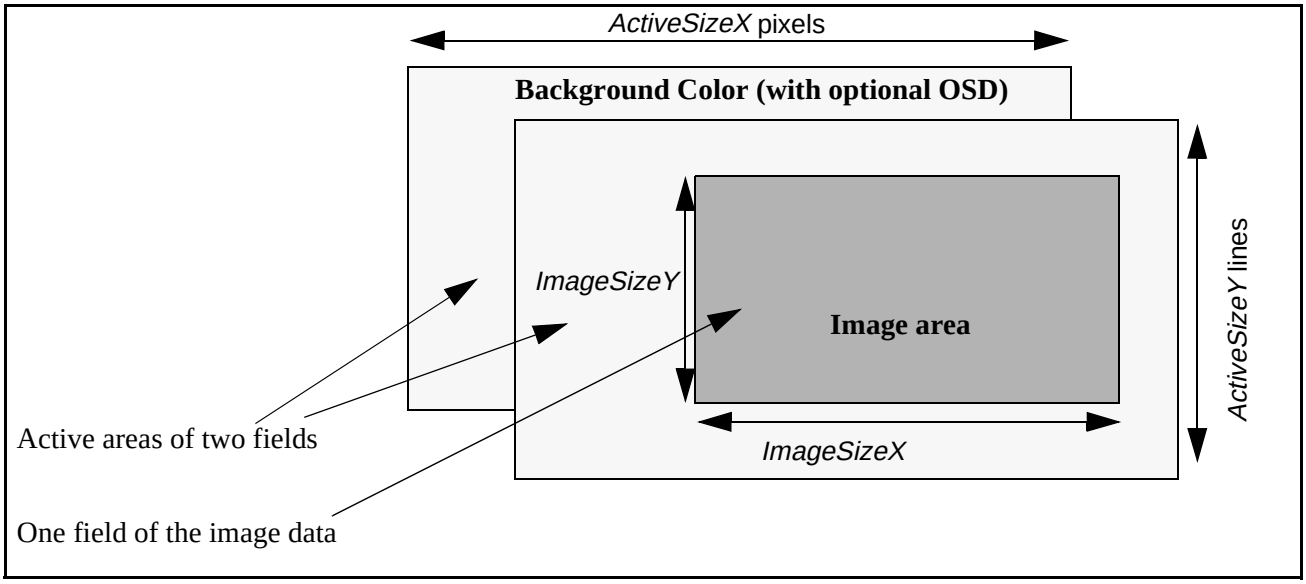

FIGURE 30. Background color is displayed within the active area, outside the image area. Sub-picture and OSD can be put in this background color region.

The host has the option of forcing the background color to black (Y = 16, U = V = 128) whenever a decoded image is displayed within the image area. This option is controlled by setting the *Black* bit of the *PlaybackMode*[1] set-up parameter to the appropriate value as shown in Table 22 .

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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TABLE 22. Forcing the Background Color to Black While Displaying a Decoded Image

***PlaybackMode* (0x41)**							
15 - 10	**9**	**8, 7**	**6**	**5**	**4**	**3**	**2 - 0**
reserved	LastPic	reserved	VidFloat	reserved	Black	DVDReqEnable	reserved
Reserved bits must be 0.							
Black	0 = The programmed background color is displayed within the active area, outside the image area. 1 = While a decoded image is displayed in the image area, the active area outside the image area is black. When a decoded image is not displayed, this region switches to the programmed background color.						

Even though the host can write any value from 0 to 255 into the *ColorY*, *ColorU* and *ColorV* parameters, the host has the option of limiting the actual background (along with the video, sub-picture and OSD) color values presented on the pixel bus as explained in Section 4.5.5 “Pixel Formats”.

4.5.5 Pixel Formats

The **ZR36710** outputs YUV 4:2:2 digital video on either an 8-bit or 16-bit pixel bus. The 8-bit format complies with the component ordering of CCIR 656 (U0, Y0, V0, Y1, U2, Y2, V2, Y3,...). The 16-bit format complies with CCIR 601 (Y0 & U0, Y1 & V0, Y2 & U2, Y3 & V2,...). The format and timing of pixels on the bus are determined by the *Video8* and *VCLKPol* bits of the *VidConfig*[1] set-up parameter as shown in Table 23 .

TABLE 23. Pixel ordering on the output pins

Video8	***VCLKPol***	**Pixel Format and Timing**
0	0	16-bit pixel bus: Y pixels on ***Y[7:0]***, UV pixels on ***C[7:0]***. Data on ***Y[7:0]*** and ***C[7:0]*** is valid on rising edge of ***VCLKx2*** when ***VCLK*** is low.
0	1	16-bit pixel bus: Y pixels on ***Y[7:0]***, UV pixels on ***C[7:0]***. Data on ***Y[7:0]*** and ***C[7:0]*** is valid on rising edge of ***VCLKx2*** when ***VCLK*** is high.
1	0	8-bit pixel bus on ***Y[7:0]***. Y pixels are valid on rising edge of ***VCLKx2*** when ***VCLK*** is low. UV pixels are valid on rising edge of ***VCLKx2*** when ***VCLK*** is high.
1	1	8-bit pixel bus on ***Y[7:0]***. Y pixels are valid on rising edge of ***VCLKx2*** when ***VCLK*** is high. UV pixels are valid on rising edge of ***VCLKx2*** when ***VCLK*** is low.

The host has the option of limiting the pixel values presented on the pixel bus by setting the *PixLim* bit of the *VidConfig* set-up parameter to the desired value as shown in Table 24 . If SAV and EAV sync codes are presented on the pixel bus as explained in Section 4.5.6 “CCIR 656 Insertion of Sync Codes on 8-bit Pixel Data”, then this bit must be set to 1.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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TABLE 24. Limiting the range of pixel values

***VidConfig* (0x01)**															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	PixLim	OSDMode	HSPol	VSPol	FIPol	FIVEdge	CBPol	VEdge	HEdge	FidSel	FidLevel	VSelect	Sync8	Video8	VCLKPol
Reserved bit 15 must be 0.															
PixLim			0 = Y, U and V pixels are limited within range of 0 to 255 inclusive. 1 = Pixel values are limited in following ranges: 16 <= Y <= 235, 16 <= U,V <= 240. Must be 1 if Sync8 = 1.												

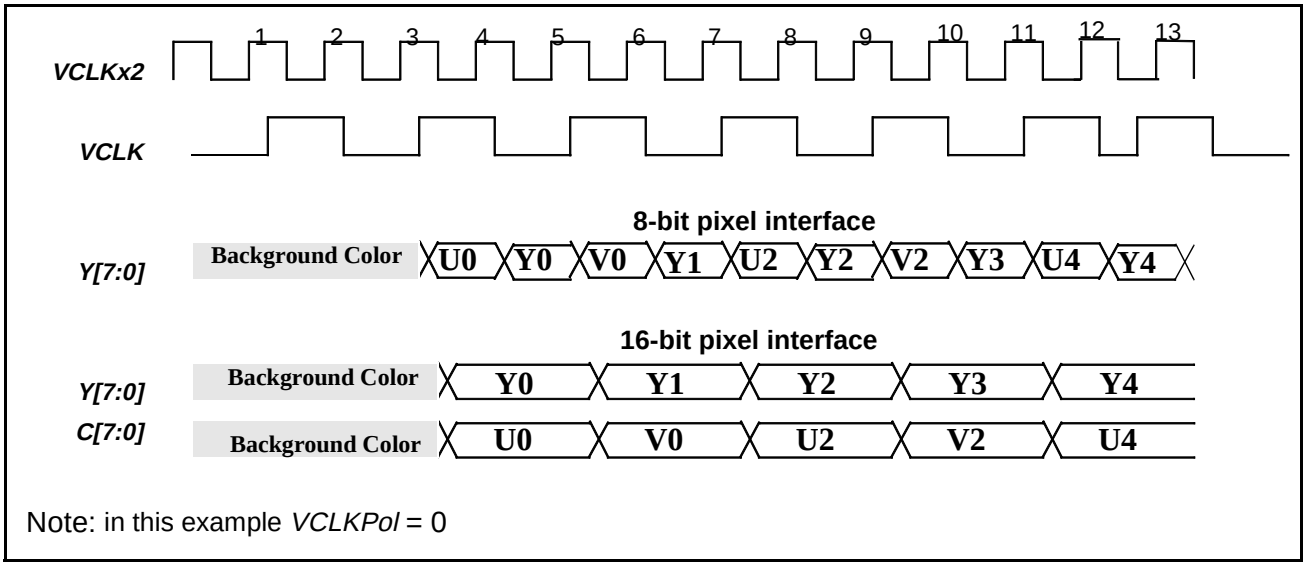

FIGURE 31. Component ordering and timing in the two video formats.

4.5.6 CCIR 656 Insertion of Sync Codes on 8-bit Pixel Data

The **ZR36710** supports insertion of SAV and EAV sync codes into the 8-bit pixel data for CCIR 656 and Video Interface Port (VIP) compliance. This support for both master and slave modes. These sync codes are known as “timing reference codes” (TRCs). Each TRC is a sequence of 4 bytes output on the ***Y[7:0]*** bus during 4 consecutive ***VCLKx2*** periods, where the first byte always replaces a U sample. There is no support for ancillary (e.g. audio) data as mentioned in the VIP 1.1 specification.

TABLE 25. Timing Reference Codes (TRCs) for CCIR 656 Support

Byte	Value on *Y[7:0]*	TRC Format
1	0xFF	Fixed marker for first byte of TRC.
2	0x00	Fixed marker for 2nd byte of TRC.
3	0x00	Fixed marker for 3rd byte of TRC.
4	TRC data	Format: Y[7] = T, Y[6] = F, Y[5] = V, Y[4] = H, Y[3] = P3, Y[2] = P2, Y[1] = P1, Y[0] = P0

Definitions

- *Field 1* (defined in CCIR 656) or *Odd Field* (defined in VIP): Defined in this data sheet as Field I, the field that begins at the beginning of a line and ends in the middle of a line.
- *Field 2* (defined in CCIR 656) or *Even Field* (defined in VIP): Defined in this data sheet as Field II, the field that begins in the middle of a line and ends at the end of a line.
- *Active video line*: Line with reconstructed MPEG video, background color, OSD or sub-picture.
- *Closed Caption line*: Line with modulated closed caption data or other modulated data.

Definitions (continued):

- *Blanking line*: Any other line not of the previous two types.
- *Stagger line*: The line whose first half belongs to field 1 and whose second half belongs to field 2.

Placement of SAV and EAV Codes

Two TRCs are output during each line. For lines with active video, one TRC (called SAV) is output just before the first active U sample. The second TRC (called EAV) is output just after the last active Y sample as shown in Figure 32.

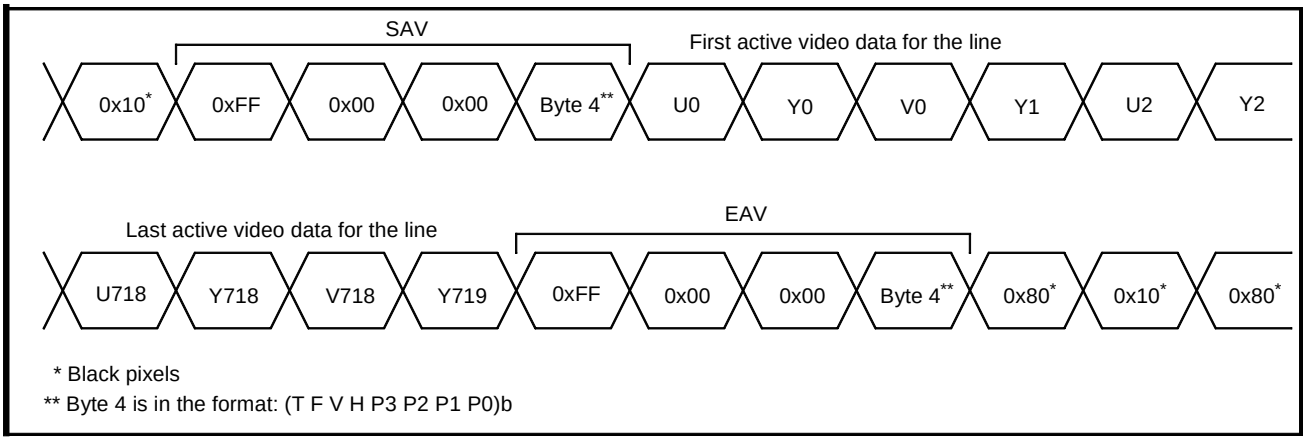

FIGURE 32. SAV and EAV for a line with 720 active pixels.

For lines without active video, the TRCs are “vertically” aligned with the TRCs of the lines with active video. The output on Y[7:0] pins immediately after the last EAV byte or after any SAV byte for a line with no active video nor closed captions data is alternating 0x80, 0x10 (black).

Definition of TRC Bits

Table 26 shows the definition of the T, F, V, H, P3, P2, P1 and P0 bits of the fourth byte of the TRC.

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TABLE 26. Definition of TRC bits

Bits	Definition
T	0 = Closed caption line. Applies for both SAV and EAV. 1 = All other lines. Applies for both SAV and EAV.
F	0 = Field 1 lines and stagger line. Applies to SAV. 1 = Field 2 lines. Applies to SAV. This bit of the EAV has the same value as the SAV of the following line.
V	0 = Active video line or closed caption line. Applies to SAV. 1 = Blank line. Applies to SAV. This bit of the EAV has the same value as the SAV of the following line.
H	0 = SAV. 1 = EAV.
P[3:0]	Error protection bits whose format is explained in Section 8.1 of the VIP 1.1 Specification.

Enable/Disable Insertion of Sync Codes

When operating in 8-bit pixel mode, the insertion of SAV and EAV codes can be enabled or disabled by writing the appropriate value to the *Sync8* bit of the *VidConfig*[1] set-up parameter as shown in Table 27 .

TABLE 27. Enable/Disable Insertion of SAV and EAV Sync Codes

***VidConfig* (0x01)**															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	PixLim	OSDMode	HSPol	VSPol	FIPol	FIVEdge	CBPol	VEdge	HEdge	FidSel	FidLevel	VSelect	Sync8	Video8	VCLKPol
Reserved bit 15 must be 0.															
Sync8			0 = Pixel bus does not contain SAV and EAV (VIP/CCIR 656) sync codes. Must be 0 if Video8 = 0. 1 = Pixel bus contains SAV and EAV (VIP/CCIR 656) sync codes.												

4.5.7 Disabling the Video Output and PIP Applications

The **ZR36710** is capable of sharing the pixel bus with other video sources. To disable the pixel bus, the system must de-assert the ***VDEN#*** input. When it is de-asserted, the **ZR36710** tri-states its Y and/or U/V outputs within 15ns. When it is asserted again, the **ZR36710** outputs its Y and/or U/V within 15ns.

If the **ZR36710** is the sync master, the following output signals are always active, regardless of ***VDEN#***:

- ***VCLK***, ***VCLKx2***, ***HSYNC***, ***VSYNC***, ***FI***, and ***CBLANK***.

1. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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In a system with two video sources using the same pixel bus, the ***CBLANK*** signal can be used to disable the **ZR36710**'s pixel bus by connecting this signal to the ***VDEN#*** pin. ***CBLANK*** could also be connected to a pixel bus mux switch. By properly defining the waveform of ***CBLANK***, both decoders can share the pixel bus which allows for picture-in-picture (PIP) support.

4.6 Audio Interface

The audio interface consists of two clocks, one frame sync, one data line input and four data output lines. These signals, ***AMCLK***, ***ABCLK***, ***ALRCLK***, ***AIN***, ***AOUT[2:0]*** and ***S/PDIF***, are explained in the following sub-sections.

4.6.1 *AMCLK* Signal

AMCLK is the master clock line, which defaults after RESET as an input pin, but must be configured as an output pin by writing the CFG[1] ADP command (a reserved bit takes care of this).

The ***AMCLK*** frequency should be equal to the reconstructed audio sampling rate (f_s) multiplied by 128, 192, 256 or 384, according to the selected audio DAC.

TABLE 28. Parameters for ***AMCLK***, ***ABCLK*** and ***ALRCLK***

Audio Port Configuration via the CFG ADP Command	
CPB, CPA (1 bit each)	0 = ***AOUT***, ***AIN*** and ***ALRCLK*** sampled on falling edge of ***ABCLK***. 1 = ***AOUT***, ***AIN*** and ***ALRCLK*** sampled on rising edge of ***ABCLK***. CPB and CPA must be set to the same value.
FRB, FRA (3 bits each)	000b = ***ALRCLK*** period is 32 ***ABCLK*** cycles. 001b = ***ALRCLK*** period is 64 ***ABCLK*** cycles. 111b = ***ALRCLK*** period is 48 ***ABCLK*** cycles. All other combinations = Reserved, do not use. FRB and FRA must be set to the same value.
SPBS (8 bits)	These bits define the ratio between the ***AMCLK*** and ***ABCLK*** rates. The allowed values are 2, 3, 4 and 6. They should be selected according to Table 29 .

4.6.2 *ABCLK* Signal

ABCLK is the output sampling clock used to indicate to a DAC when the output (both data and frame sync, explained below) is valid to sample and also when the **ZR36710** samples incoming audio data (e.g. karaoke, explained below). The sampling edge of ***ABCLK*** is selectable by the *CPB* and *CPA* bits of the CFG ADP command as shown in Table 28 .

The frequency of ***ABCLK*** is derived by dividing ***AMCLK*** with the value of the *SPBS* bits of the CFG ADP command. ***ABCLK*** is dependent on the period of the frame sync output (explained below), and *SPBS* should be selected according to Table 29 .

1. See Section 12.4 "Set-up Commands" for an explanation on configuring the audio port via the CFG ADP command.

TABLE 29. *SPBS* bits of the CFG ADP Command

AMCLK/f_S	***ALRCLK*** period	*SPBS*
128	32	2
192	32	3
192	48	2
256	64	2
256	32	4
384	48	4
384	64	3
384	32	6

4.6.3 *ALRCLK* Signal

ALRCLK is the frame synchronization output line. This signal should be sampled by a DAC on the selected sampling edge of ***ABCLK***. The period of ***ALRCLK*** can be 32, 48 or 64 ***ABCLK*** cycles as selected by the *FRB* and *FRA* bits of the CFG[1] ADP command as shown in Table 28 .

4.6.4 Input and Output Data - *AIN*, *AOUT[2:0]* and *S/PDIF*

Input Signals - *AIN*

AIN, is a two-channel input line whose data is sampled into the **ZR36710** on the selected sampling edge of ***ABCLK***. For karaoke applications, this signal is provided via a microphone ADC.

Output Signals - *AOUT[2:0] and S/PDIF*

AOUT[2:0] and ***S/PDIF*** are four data output lines whose data (excluding ***S/PDIF***) should be sampled by a DAC on the selected sampling edge of ***ABCLK***. Two channels of audio are transmitted on each of the ***AOUT[2:0]*** lines, allowing for 6 channels. The *SPO* bit of the CFG ADP command determines whether the ***S/PDIF*** pin operates as a S/PDIF transmitter or as a fourth 2-channel data line, ***AOUT[3]***, allowing 8-channel audio output as shown in Table 30 .

1. See Section 12.4 “Set-up Commands” for an explanation on configuring the audio port via the CFG ADP command.

TABLE 30. Parameters for ***AIN***, ***AOUT[2:0]*** and ***S/PDIF***

Audio Port Configuration via the CFG and SPDIFCS ADP Commands	
OSP (1 bit) (CFG ADP command)	0 = ***ALRCLK*** low indicates the left channel for data on ***AOUT***. ***ALRCLK*** high indicates the right channel. 1 = ***ALRCLK*** high indicates the left channel for data on ***AOUT***. ***ALRCLK*** low indicates the right channel.
ISP (1 bit) (CFG ADP command)	0 = ***ALRCLK*** low indicates the left channel for data on ***AIN***. ***ALRCLK*** high indicates the right channel. 1 = ***ALRCLK*** high indicates the left channel for data on ***AIN***. ***ALRCLK*** low indicates the right channel.
OUTW (2 bits) (CFG ADP command)	00b = ***AOUT*** is 20 bits wide. 01b = ***AOUT*** is 18 bits wide. 10b = ***AOUT*** is 16 bits wide. 11b = ***AOUT*** is 24 bits wide. Only applicable if a single stereo pair is output on ***AOUT[0]***.
INW (2 bits) (CFG ADP command)	00b = ***AIN*** is 20 bits wide. 01b = ***AIN*** is 18 bits wide. 10b = ***AIN*** is 16 bits wide. 11b = ***AIN*** is 24 bits wide.
FMB (3 bits) (CFG ADP command)	00b = ***AOUT*** is left-justified with ***ALRCLK***. 01b = ***AOUT*** is left-justified with ***ALRCLK***, with a delay of one ***ABCLK*** cycle. 10b = ***AOUT*** is right-justified with ***ALRCLK***. All other combinations = Reserved, do not use.
FMA (3 bits) (CFG ADP command)	000b = ***AIN*** is left-justified with ***ALRCLK***. 001b = ***AIN*** is left-justified with ***ALRCLK***, with a delay of one ***ABCLK*** cycle. 111b = ***AIN*** is right-justified with ***ALRCLK***. All other combinations = Reserved, do not use.
SPO (1 bit) (CFG ADP command)	0 = ***S/PDIF*** pin acts as ***AOUT[3]***, a fourth reconstructed stereo output. 1 = ***S/PDIF*** pin acts as S/PDIF transmitter.
data mode (bit #1 of the channel status value of the SPDIFCS ADP command)	0 = ***S/PDIF*** transmitter outputs reconstructed stereo. Must be 0 if *SPO* = 0 or if not applicable. 1 = ***S/PDIF*** transmitter outputs coded audio data.

When ***S/PDIF*** is configured as a S/PDIF transmitter, the output can be either the coded audio stream or reconstructed two-channel PCM audio according to the IEC 958 specs (please refer to this document for timing diagrams of the S/PDIF output). The *data mode* bit of SPDIFCS[1] ADP command indicates the output mode as shown in Table 30 .

Data Width - 16, 18, 20 or 24 Bits Per Data Word

The data on the ***AOUT*** lines is organized as words with a width specified by the *OUTW* bits of the CFG[1] ADP command. The data on the ***AIN*** line is organized as words with a width specified by the *INW* bits of the CFG ADP command. These parameters are described in Table 30 .

1. See Section 12.4 “Set-up Commands” for an explanation on configuring S/PDIF via the SPDIFCS ADP command.

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Word Alignment - Left-Justified, Left-Justified + one *ABCLK* or Right-Justified

Each word (both output and input) is sampled between two transitions of the ***ALRCLK*** signal. Data is presented m.s. bit first. The words align with the transition of ***ALRCLK*** as defined by the *FMB* (output) and *FMA* (input) bits of the CFG[1] ADP command as described in Table 30 .

Left-justified is defined as the m.s. bit of the word is sampled immediately after the transition of the ***ALRCLK*** signal. Right-justified is defined as the l.s. bit of the word is sampled immediately prior to the transition of the ***ALRCLK*** signal.

If the data is organized as 16-bit words and the period of ***ALRCLK*** is 32 ***ABCLK*** cycles and the first bit of each word is sampled one ***ABCLK*** cycle after the transition of the ***ALRCLK*** signal, then the last bit of the word will appear after the next transition of the ***ALRCLK*** signal. This is because the transition of ***ALRCLK*** occurs every 16 ***ABCLK***s. The same is true for 24-bit words and an ***ALRCLK*** period of 48.

If the word width is less than the number of ***ABCLK*** cycles between transitions of ***ALRCLK***, then the following holds true during the “spare” clock cycles:

- Left-justified: After presentation of the entire word, the output (input) is zero.
- Right-justified: The m.s. bit of the word is repeated until the word is aligned.

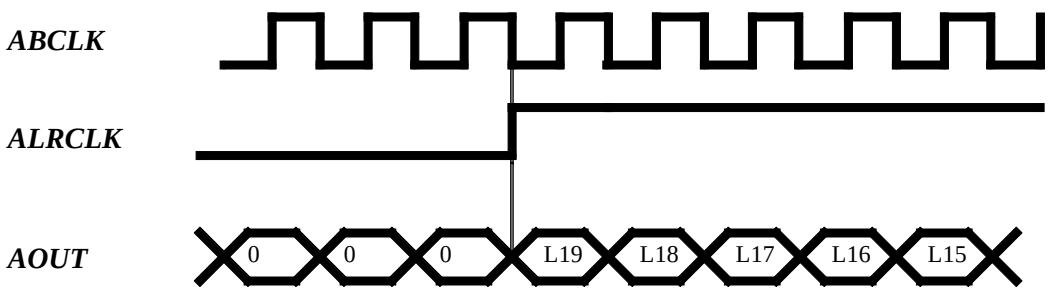
Left and Right Channel Determination Per Data Line

On the ***AOUT*** and ***AIN*** lines, words of left-channel audio data are alternating with words of right-channel audio data. The left channel on the ***AOUT*** line is output either when the level of the ***ALRCLK*** signal is high or low, as specified by the *OSP* bit of the CFG ADP command. The left channel on the ***AIN*** line is input either when the level of the ***ALRCLK*** signal is high or low, as specified by the *ISP* bit of the CFG ADP command as explained in Table 30 .

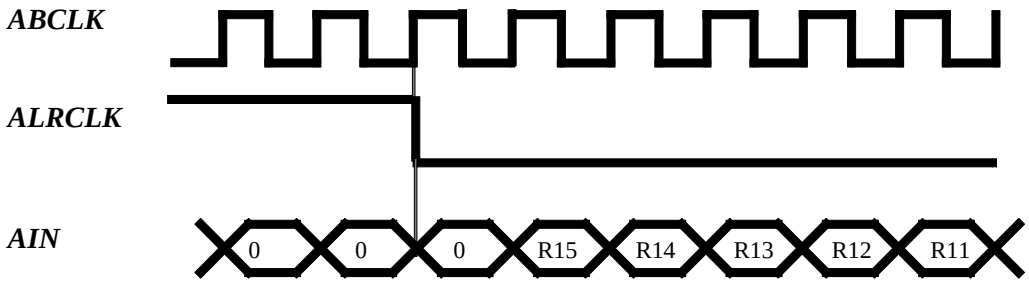
4.6.5 Timing Diagrams for the Audio Interface

Figure 18 and Figure 19 in Section 4.4 “DVD-DSP and CD-DSP Interfaces” also double as an example for interface timing of the audio interface for 16-bit words (the CD-DSP interface is almost identical to the audio interface). The following figures provide further examples.

1. See Section 12.4 “Set-up Commands” for an explanation on configuring the audio port via the CFG ADP command.



ALRCLK period is 48, word length is 20 bits, left justified, signals should be sampled with the rising edge of ***ABCLK***, left channel = high ***ALRCLK***.



ALRCLK period is 48 or 64, word length is 16 bits, left justified + ***ABCLK*** period, signals should be sampled with the falling edge of ***ABCLK***, left channel = high ***ALRCLK***.

FIGURE 33. Audio interface signals (Examples)

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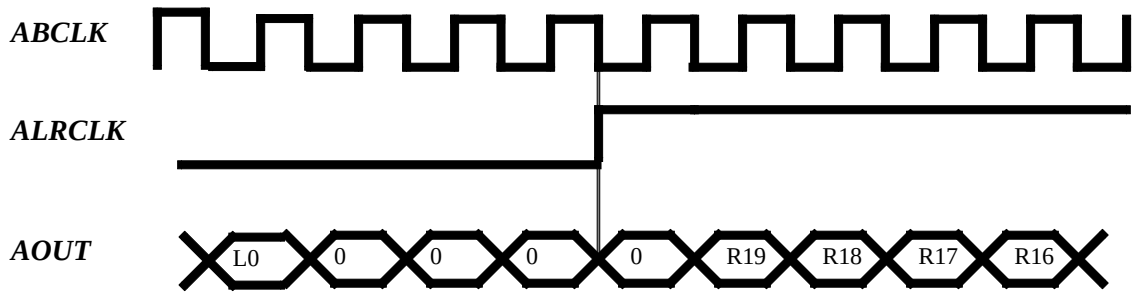
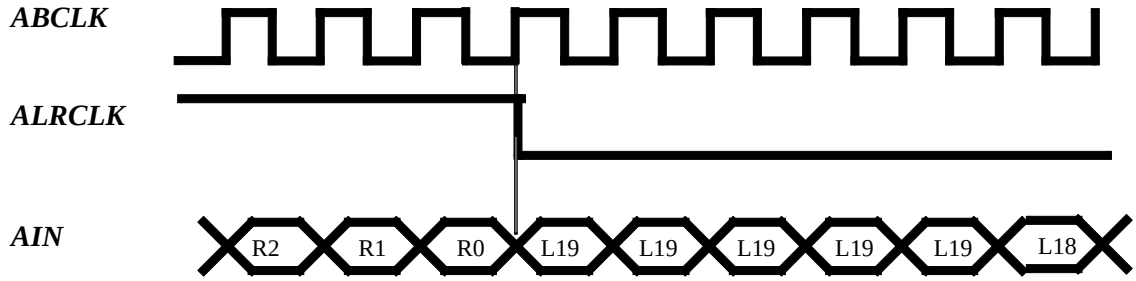


ALRCLK period is 48, word length is 20 bits, left justified + ***ABCLK*** period, signals should be sampled with the falling edge of ***ABCLK***, left channel = low ***ALRCLK***.



ALRCLK period is 48 word length is 20 bits, right justified signals should be sampled with the falling edge of ***ABCLK,*** left channel = low ***ALRCLK***.

FIGURE 34. Audio interface signals (Examples, cont.)

5. Host Software Interface - Register Access

Section 4.3.3 “Address/Register Space and Register Access” introduces the register map of the **ZR36710**. The address space translates into 16 readable and writable 16-bit registers. It is through these registers that the host configures, controls and monitors the device. This section describes the software specification of these registers. For an explanation of the hardware specification (e.g. 8-bit versus 16-bit host data transfers), please refer to Section 4.3.3 “Address/Register Space and Register Access”.

5.1 General Set-up Parameters and Microcode - Reg. 0x0 and 0x1

The set-up parameters (excluding the ADP command-related parameters as described in Section 12. “Annex A: ADP Commands”) and DVP microcode that are used to configure the **ZR36710** are loaded/ read via registers 0x0 and 0x1.

TABLE 31. ZR36710 General Set-up Parameter/Microcode Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

General set-up parameters must be loaded into the **ZR36710** to configure the device for even the most basic of functions such as generating video sync signals or creating audio clocks to an audio DAC at the right frequency. Microcode must be loaded prior to issuing a **start**[1] host command to the device.

1. See Section 6.11 “Host Commands and Control over the Playback Operation” for an explanation on loading host commands to the **ZR36710**.

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5.1.1 General Set-up Parameter Access Protocol

The general set-up parameters are arranged in an internal indexed address space. Table 32 explains the access protocol to these indexed addresses.

TABLE 32. General Set-up Parameter Access Protocol

Sequence of ZR36710 Accesses to Write General Set-up Parameters
1. Write the 8-bit parameter indexed address to the l.s. byte of the Parameter Address Register. The m.s byte must be set to 0x00.
2. Write/read the 16-bit parameter data to/from the Parameter Data Register.
3. If the parameter indicated by the indexed address requires multiple 16-bit values, then the host must execute consecutive writes to/reads from the Parameter Data Register without updating the Parameter Address Register for each word. In the case of writing/reading multiple words from an indexed address, data is transferred m.s. word first.
Note: Reading the Parameter Address Register simply results in the last value (indexed address) that was written to this register. Only a small portion of the parameters can be read back by the host.

Some of the parameter bits have default values which are preset to a given value during RESET. The default values are needed to specify input signal directions for bidirectional lines to avoid contention. These default bits value are indicated with the description of each bit in this section. All other parameters do not have default values and should be loaded (at the appropriate stage) before used. Reserved bits must be written as zeros. For parameters that can be read, reserved bit values are not guaranteed. Reserved addresses must not be written to nor read from.

Only some of the parameters are readable. The host must never attempt to read any parameters that are not readable. If the host attempts to read parameters that are not designated as readable, the ***HACK#*** signal on the host bus will not be de-asserted, effectively hanging the host interface.

5.1.2 General Set-up Parameter List

Table 34 lists the general set-up parameters, and specifies for each parameter its hexadecimal indexed address, width in bytes, name, description and the initialization stage (see Table 33) in which it has to be loaded with an indication if it can be changed during playback. All parameters are writable, but parameters designated by “RW” in the width column can also be read back by the host. Unless otherwise specified, all 16-bit parameters (e.g. *ActiveStartX*, *ImageSizeY*) are treated as 16-bit unsigned integers.

TABLE 33. Initialization Stages of the **ZR36710**

Stage	Function
Stage 1	Immediately after RESET. This stage involves locking the ***PCLK*** portion of the PLL as explained in Section 4.2 “Phase-Locked Loop Interface”.
Stage 2	**C-STATE**[a] = ***init_pclk***. Once ***PCLK*** is stabilized, but before **C-STATE** = ***init_display*** as explained in Section 14.2 “Stage 2: I/O Port Configuration”.
Stage 3	**C-STATE** = ***init_display*** or ***Idle***. Preparation for playback.
Playback	**C-STATE** != ***Idle***, ***reset***, ***init_pclk*** nor ***init_display***. Playback is taking place.

a. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

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TABLE 34. General Set-up Parameters

Index Addr.	Width in Bytes	Parameter Name	Description	Initialization stage
0x00	2	*SysConfig*	System configuration	**C-STATE** = ***init_pclk***
01	2 RW	*VidConfig*	Video port configuration	**C-STATE** = ***init_pclk***
02	2	*SDConfig*	DVD-DSP/CD-DSP port configuration	**C-STATE** = ***init_pclk***
03	2	*DVPGen1*	General purpose DVP data input parameter 1	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** with option to change during playback.
04	2	*DVPGen2*	General purpose DVP data input parameter 2	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** with option to change during playback.
05	2	*DVPGen3*	General purporse DVP data input parameter 3	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** with option to change during playback.
...		Reserved		
08	2 RW	*ColorV*	V component of the background color	**C-STATE** = ***init_pclk***, with option to change any time after
09	2 RW	*ColorY*	Y component of the background color	**C-STATE** = ***init_pclk***, with option to change any time after
0A	2 RW	*ColorU*	U component of the background color	**C-STATE** = ***init_pclk***, with option to change any time after
...		Reserved		
10	2	*VidOut*	Display frame rate and field selections	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
11	2 RW	*Htotal*	Number of total pixels per line	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
12	2 RW	*Vtotal*	Number of total lines per display frame	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
13	2 RW	*HSyncSize*	Width of horizontal sync signal (pixels)	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
14	2 RW	*VSyncSize*	Width of vertical sync signal (lines)	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
15	2 RW	*CBHStart*	Number of initial blank pixels per line	**C-STATE** = ***init_pclk*** and/or any time after
16	2 RW	*CBVStart*	Number of initial blank lines per field	**C-STATE** = ***init_pclk*** and/or any time after

TABLE 34. General Set-up Parameters

Index Addr.	Width in Bytes	Parameter Name	Description	Initialization stage
17	2 RW	*CBHEnd*	Number of initial blank plus non-blank pixels per line	**C-STATE** = ***init_pclk*** and/or any time after
18	2 RW	*CBVEnd*	Number of initial blank plus non-blank lines per field	**C-STATE** = ***init_pclk*** and/or any time after
19	2 RW	*ActiveStartX*	Number of initial non-active pixels per line	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
1A	2 RW	*ActiveStartY*	Number of initial non-active lines per field	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
1B	2 RW	*ActiveEndX*	Number of initial non-active plus active pixels per line	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
1C	2 RW	*ActiveEndY*	Number of initial non-active plus active lines per field	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***.
1D	2 RW	*ActiveSizeX*	Number of active pixels per line	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***.
1E	2 RW	*ActiveSizeY*	Number of active lines per picture or field	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
1F	2 RW	*CaptionOffset*	Number of offset lines for the closed captions data insertion	**C-STATE** = ***init_pclk***, with option to change while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
20	2	*StartDisplay*	Switch in a new (or modified) set of video output parameters	**C-STATE** = ***init_pclk***, with option to write while **C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
...		Reserved		
28	2 RW	*OSDControl*	OSD configuration	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
29	2	*OSDMemStart*	Number of offset bytes between the starting address of the OSD plane and starting of OSD overlay data	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
2A	2	*OSDMemSize*	Size in bytes of the OSD overlay data	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
2B	2 RW	*OSDFirstLine*	First line enabled for OSD overlay	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
2C	2 RW	*OSDLastLine*	Last line enabled for OSD overlay	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback

TABLE 34. General Set-up Parameters

Index Addr.	Width in Bytes	Parameter Name	Description	Initialization stage
2D	2	*OSDSwitch*	Switch OSD display on and off	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
...		Reserved		
30	4	*SCLKValue*	**SCLK** comparison value for interrupt	During playback
...		Reserved		
38	2	*DiscType*	Disc type indication	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
...		Reserved		
40	2	*BitstreamSelect*	Bitstream selection	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
41	2	*PlaybackMode*	Playback mode	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
42	2	*AudSID*	Audio stream (or sub-stream) I.D.	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
43	2	*VidSID*	Video stream I.D.	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
44	2	*SPSID*	Sub-picture (sub-stream) I.D.	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
45	2	*AudPortDelay*	Audio port delay (**SCLK** units)	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
46	2	*VidPortDelay*	Video port delay (**SCLK** units)	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
47	2	*VidTolerance*	Video synchronization tolerance (**SCLK** units)	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
48	2	*VidSyncMode*	Video synchronization mode selection	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
49	64	*SPPalette*	Color and transparency LUT for sub-picture	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
...		Reserved		
50	2	*AutoScaling*	Video post-processing parameter group calculating entity	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
51	2	*PanScanBaseX*	Number of base offset pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
52	2	*PanScanBaseY*	Number of base offset lines per picture or field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
53	2	*PanScanSizeX*	Number of processed image pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
54	2	*PanScanSizeY*	Number of processed image lines per picture or field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback

TABLE 34. General Set-up Parameters

Index Addr.	Width in Bytes	Parameter Name	Description	Initialization stage
55	2 RW	*PicSizeX*	Number of pixels per line after fixed scaler - 1	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
56	2 RW	*PicSizeY*	Number of lines per field after fixed scaler - 1	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
57	2 RW	*ImageStartX*	Number of initial background pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
58	2 RW	*ImageStartY*	Number of initial background lines per field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
59	2 RW	*ImageSizeX*	Number of output image pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
5A	2 RW	*ImageSizeY*	Number of output image lines per field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
5B	2 RW	*ImageEndX*	Number of initial background plus output image pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
5C	2 RW	*ImageEndY*	Number of initial background plus output image lines per field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
5D		Reserved		
5E	2	*ScaleRatio*	Horizontal and vertical scaling ratios	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
5F	2	*SPScale*	Sub-picture vertical scaling selection	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
...		Reserved		
68	2	*AutoPanScan*	PanScan offset parameter group calculating entity	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
69	2	*PanScanOffsetX*	Number of relative offset pixels per line	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
6A	2	*PanScanOffsetY*	Number of relative offset lines per picture or field	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
6B	2	*BackGroundSwitch*	Switch video output between background and reconstructed image	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
6C	2	*SPSwitch*	Switch sub-picture display	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
6D	2	*CaptionWord*	Closed Captions host data	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
6E		Reserved		
6F	2	*CaptionSwitch*	Switch Closed Captions display	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback

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TABLE 34. General Set-up Parameters

Index Addr.	Width in Bytes	Parameter Name	Description	Initialization stage
70	6	*HiLightButton1*	Button 1 geometrical data	During playback
71	6	*HiLightButton2*	Button 2 geometrical data	During playback
72	8	*HiLightColor1*	Active Button highlight color (1 of 3)	During playback
73	12	*HiLightTiming*	Active Button highlight timing	During playback
74	2	*HiLightSwitch*	Switch highlight display and mode	During playback
75	8	*HiLightColor2*	Active Button highlight color (2 of 3)	During playback
76	8	*HiLightColor3*	Active Button highlight color (3 of 3)	During playback
...		Reserved		
80 -8F	16x4	*OSDPalette0i* i = 0 to 15	Color and transparency for index i in LUT No. 0 for OSD	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
90 -9F	16x4	*OSDPalette1i* i = 0 to 15	Color and transparency for index i in LUT No. 1 for OSD	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
...		Reserved		
CE	2	*DVPCmd*	Host command to DVP	During playback
CF	2	*DecCntr*	Indicates no further need for a NAV segment	During playback
...		Reserved		
E0	2	DynPanX	Dynamic Panning X offset	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
E1	2	DynPanY	Dynamic Panning Y offset	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle*** and/ or during playback
...		Reserved		
F0	variable	(init file)	Initialization (Init) file #1	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
F1	variable	(init file)	Init file #2	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
F2	variable	(init file)	Init file #3	**C-STATE** = ***init_display***, **C-STATE** = ***init_pclk*** or **C-STATE** = ***Idle***, but only once after each RESET
F3	variable	(init file)	Init file #4	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
...		Reserved		
FD	variable	(microcode)	DVP microcode	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***
FE		Reserved		
FF		Reserved		

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The following tables give the structure for each of the general set-up parameters listed above. For parameters that have names for their bits, the bit number(s) is assigned to the names of these bits.

***SysConfig* (0x00)**						
15, 14	**13**	**12**	**11 - 4**	**3**	**2**	**1, 0**
reserved	NumDRAMDev	CodeSource	CodBurstLen	DecBypass	HACKMode	reserved

Reserved bits must be 0.	
NumDRAMDev	0 = 1 16Mbit SDRAM. 1 = 2 16Mbit SDRAMs.
CodeSource	0 = DVD-DSP/CD-DSP interface provides bitstream data. 1 = Host bus interface provides bitstream data.
CodBurstLen	If CodeSource = 0, allowed values are 16, 32, 64. If CodeSource = 1, allowed values are 4, 8, 16, 32, 64.
DecBypass	0 = Internal decryption circuit is disabled (bypass). 1 = Internal decryption circuit is enabled.
HACKMode	0 = HACK# operates in default mode. 1 = In Type B transfers to the Coded Bitstream Register (Register 0x4), HACK# will not activate until HRDY is active.

***VidConfig* (0x01)**															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	PixLim	OSDMode	HSPol	VSPol	FIPol	FIVEdge	CBPol	VEdge	HEdge	FidSel	FidLevel	VSelect	Sync8	Video8	VCLKPol

Reserved bit 15 must be 0.	
PixLim	0 = Y, U and V pixels are limited within range of 0 to 255 inclusive. 1 = Pixel values are limited in following ranges: 16 <= Y <= 235, 16 <= U,V <= 240. Must be 1 if Sync8 = 1.
OSDMode	0 = Internal OSD mode. 1 = External OSD mode, Video8 must be set to 1.
HSPol	0 = HSYNC active-low in master mode. Must be 0 in slave mode. 1 = HSYNC active-high in master mode.
VSPol	0 = VSYNC active-low in master mode. Must be 0 in slave mode. 1 = VSYNC active-high in master mode.
FIPol	0 = FI is low during Field I, high during Field II in master mode. Must be 0 in slave mode. 1 = FI is high during Field I, low during Field II in master mode.
FIVEdge	0 = FI toggles on leading edge of VSYNC in master mode. Must be 0 in slave mode. 1 = FI toggles on trailing edge of VSYNC in master mode.
CBPol	0 = CBLANK is active-low. 1 = CBLANK is active-high.
VEdge	0 = Falling edge of VSYNC is effective edge. 1 = Rising edge of VSYNC is effective edge.
HEdge	0 = Falling edge of HSYNC is effective edge. 1 = Rising edge of HSYNC is effective edge.

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***VidConfig* (0x01)**															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	PixLim	OSDMode	HSPol	VSPol	FIPol	FIVEdge	CBPol	VEdge	HEdge	FidSel	FidLevel	VSelect	Sync8	Video8	VCLKPol

Reserved bit 15 must be 0.	
FidSel	0 = Field indication uses FI signal level on effective edge of VSYNC. 1 = Field indication uses HSYNC signal level on effective edge of VSYNC. Must be 1 if number of lines for both fields is even.
FidLevel	0 = Field I is indicated by effective edge of VSYNC sampling FI or HSYNC low. 1 = Field I is indicated by effective edge of VSYNC sampling FI or HSYNC high.
VSelect	0 = Field II line counting starts with 0. 1 = Field II line counting starts with 1.
Sync8	0 = Pixel bus does not contain SAV and EAV (VIP/CCIR 656) sync codes. Must be 0 if Video8 = 0. 1 = Pixel bus contains SAV and EAV (VIP/CCIR 656) sync codes.
Video8	0 = Pixel bus is 16 bits. Y data on Y[7:0] and UV data on C[7:0]. 1 = Pixel bus is 8 bits. YUV data on Y[7:0].
VCLKPol	0 = Rising edge of VCLKx2 is qualified by VCLK low (syncs and 16-bit pixels). If Video8 = 1, Y data is output with VCLK low. 1 = Rising edge of VCLKx2 is qualified by VCLK high (syncs and 16-bit pixels). If Video8 = 1, Y data is output with VCLK high.

***SDConfig* (0x02)**														
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.

Reserved bit 0 must be 0.	
DVDREQSync	0 = DVDREQ operates asynchronously with DVDSTRB. Must be 0 if not applicable. 1 = DVDREQ is synchronized to DVDSTRB.
IFMode	0 = DVD-DSP interface used for CD data. Must be 0 if host bus interface is used to transfer bitstream. 1 = CD-DSP interface used. ***HWID*** = GND.
CDEdge	0 = CD-DSP interface signals are sampled on falling edge of CDCLK. Must be 0 if not applicable. 1 = CD-DSP interface signals are sampled on rising edge of CDCLK.
CDJust	00b = CDDAT data is left-justified. Must be 00b if not applicable. 01b = CDDAT data is left-justified with one CDCLK cycle delay. 10b = CDDAT data is right-justified. 11b = Reserved, do not use.
CDPeriod	00b = CDFRM period is 32 CDCLK cycles. Must be 00b if not applicable. 01b = CDFRM period is 48 CDCLK cycles. 10b = CDFRM period is 64 CDCLK cycles. 11b = Reserved, do not use.
REQPol	0 = DVDREQ is active-low. Must be 0 if not applicable. 1 = DVDREQ is active-high.
VALIDPol	0 = DVDVALID is active-low. Must be 0 if not applicable. 1 = DVDVALID is active-high.

***SDConfig* (0x02)**													
15	**14**	**13**	**12, 11**	**10**	**9, 8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DVDREQSync	IFMode	CDEdge	CDJust	res.	CDPeriod	res.	REQPol	VALIDPol	SOSPol	STRBPol	res.	CDBitSwap	res.
Reserved bits must be 0.													
SOSPol	0 = DVDSOS is active-low. Must be 0 if not applicable. 1 = DVDSOS is active-high.												
STRBPol	0 = DVD-DSP signals are sampled on falling edge of DVDSTRB. Must be 0 if not applicable. 1 = DVD-DSP signals are sampled on rising edge of DVDSTRB.												
CDBitSwap	0 = No bit swapping on CD-DSP interface. Must be 0 if not applicable. 1 = Bit swapping (reverse order l.s. to m.s.) per word on CD-DSP interface.												

***DVPGen1* (0x03)**	
DVPGen1	General DVP Data Input Parameter 1. As explained in this document, this parameter sets the frame display period in fast search mode. Refer to the microcode release notes for further definitions of this parameter.

***DVPGen2* (0x04)**	
DVPGen2	General DVP Data Input Parameter 2. As explained in this document, this parameter is used in NV_PCK retrieval, error concealment, fast search mode, automatic aspect ratio conversion and random access in special VideoCD streams. Refer to the microcode release notes for further definitions of this parameter.

***DVPGen3* (0x05)**			
15 - 2		**1**	**0**
reserved		Force Interlace	Force Progressive
Reserved bits must be 0.			
Force Interlace	0 = Use data from bitstream to determine interpolation method. Must be 0 if Force Progressive = 1. 1 = Force interlaced picture interpolation method.		
Force Progressive	0 = Use data from bitstream to determine interpolation method. Must be 0 if Force Interlace = 1. 1 = Force progressive picture interpolation method.		

***ColorV* (0x08), *ColorY* (0x09), *ColorU* (0x0A)**	
ColorV	8-bit V component of the background color. The m.s. 8 bits must be 0x00.
ColorY	8-bit Y component of the background color. The m.s. 8 bits must be 0x00.
ColorU	8-bit U component of the background color. The m.s. 8 bits must be 0x00.

***VidOut* (0x10)**			
15 - 2		**1**	**0**
reserved		FieldSel	VidFPS
Reserved bits must be 0.			
FieldSel	0 = Top field is output during Field I. Bottom field is output during Field II. 1 = Bottom field is output during Field I. Top field is output during Field II.		
VidFPS	0 = Output frame rate is 29.97 (30/1.001) frames per second - NTSC. 1 = Output frame rate is 25 frames per second - PAL.		

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***Htotal* (0x11), *Vtotal* (0x12), *HSyncSize* (0x13), *VSyncSize* (0x14)**	
Htotal	Total number of pixels/line = number of VCLKs between leading edges of consecutive HSYNC pulses. Must be even. Maximum value is 1022. Must be 0x0000 in slave mode.
Vtotal	Total number of lines/display frame = number of HSYNC pulses between every other leading edge of VSYNC. Maximum value is 1023. Vtotal x Htotal x frame rate (30/1.001 or 25) = f_{VCLK}. Must be 0x0000 in slave mode.
HSyncSize	Width (in pixels) of HSYNC active pulse in master mode. Minimum value is 8. Maximum value is (Htotal/2 - 1). Must be 0x0000 in slave mode.
VSyncSize	Width (in lines) of VSYNC active pulse in master mode. Minimum value is 1. Maximum value is (Vtotal/2 - 1). Must be 0x0000 in slave mode.

***CBHStart* (0x15), *CBVStart* (0x16), *CBHEnd* (0x17), *CBVEnd* (0x18)**	
CBHStart	Defines the number of blank pixels at the beginning of each line, measured in the number of VCLKs after the effective edge of HSYNC. Minimum value of 6. Maximum value of (CBHEnd - 1).
CBVStart	Defines the number of blank lines at the beginning of each field, measured in the number HSYNC pulses after the effective edge of VSYNC. Minimum value of 2. Maximum value of (CBVEnd - 1).
CBHEnd	Defines the blanking period at the end of each line such that there are (Htotal - CBHEnd) blank pixels at the end of each line, measured in the number of VCLKs after the effective edge of HSYNC. Minimum value of (CBHStart + 1). Maximum value of (Htotal - 1).
CBVEnd	Defines the blanking period at the end of each field such that there are (int(Vtotal/2) - CBVEnd) blank lines at the end of each field, measured in the number of HSYNC pulses after the effective edge of VSYNC. Minimum value of (CBVStart + 1). Maximum value of (int(Vtotal/2) - 1).

***ActiveStartX* (0x19), *ActiveStartY* (0x1A), *ActiveEndX* (0x1B), *ActiveEndY* (0x1C), *ActiveSizeX* (0x1D), *ActiveSizeY* (0x1E)**	
ActiveStartX	Defines the number of non-active pixels at the beginning of each line, measured in the number of VCLKs after the effective edge of HSYNC. Must be even. Minimum value of 40. Maximum value of (ActiveEndX - 2).
ActiveStartY	Defines the number of non-active lines at the beginning of each field, measured in the number of HSYNC pulses after the effective edge of VSYNC. Minimum value of 4. Maximum value of (ActiveEndY - 1).
ActiveEndX	Defines the number of non-active pixels at the end of each line such that there are (Htotal - ActiveEndX) non-active pixels at the end of each line, measured in the number of VCLKs after the effective edge of HSYNC. Must allow ActiveSizeX to be a multiple of 8. Minimum value of (ActiveStartX + 2). Maximum value of (Htotal - 2).
ActiveEndY	Defines the number of non-active lines at the end of each field such that there are (int(Vtotal/2) - ActiveEndY) non-active lines at the end of each field, measured in the number of HSYNC pulses after the effective edge of VSYNC. Minimum value of (ActiveStartY + 1). Maximum value of (int(Vtotal/2) - 1).
ActiveSizeX	Defines the number of active pixels per line. Calculated by the host, it should be (ActiveEndX - ActiveStartX) and must be a multiple of 8.
ActiveSizeY	Defines the number of active lines per field. Calculated by the host, it should be (ActiveEndY - ActiveStartY).

***CaptionOffset* (0x1F)**	
CaptionOffset	Number of lines (HSYNC pulses) after effective edge of VSYNC after which closed caption data is placed. Min. value of 2. Max. value of 31. This indicates the closed caption line.

***StartDisplay* (0x20)**	
StartDisplay	Reset all video counters and operate video interface according to values in parameters 0x00 - 0x1F. The value itself written is ignored by the **ZR36710**.

***OSDControl* (0x28)**			
15	**14, 13**	**12**	**11 - 0**
OSDMem	OSDSwitchPlane	OSDDot	reserved
Reserved bits must be 0.			
OSDMem	0 = OSD buffer is organized as one plane. 1 = OSD buffer is organized as two planes of equal size.		
OSDSwitchPlane	00b = OSD planes are switched every field. Must be 00b if OSDMem = 0. 01b = OSD planes are switched every display frame (2 fields). 10b = OSD is switched to plane 0. 11b = OSD is switched to plane 1.		
OSDDot	0 = OSD palette index (4 bits) is defined for each pixel. 1 = OSD palette index (4 bits) is defined for each horizontal pair of pixels.		

***OSDMemStart* (0x29), *OSDMemSize* (0x2A), *OSDFirstLine* (0x2B), *OSDLastLine* (0x2C)**	
OSDMemStart	Defines the number of bytes from the beginning of each OSD plane buffer to the beginning of the OSD data to be presented on the lines indicated by OSDFirstLine through OSDLastLine. Must be even.
OSDMemSize	Defines the number of bytes of each OSD plane to be presented on the lines indicated by OSDFirstLine through OSDLastLine. Must be even.
OSDFirstLine	Defines the number of active lines from the start of the active area to before the first active line for which the OSD data is enabled. Minimum value of 0. Maximum value of ActiveSizeY.
OSDLastLine	Defines the number of active lines from the start of the active area to before the last active line for which the OSD data is enabled. Minimum value of OSDFirstLine. Maximum value of ActiveSizeY.

***OSDSwitch* (0x2D)**	
15 - 1	**0**
reserved	OSDSwitch
Reserved bits must be 0.	
OSDSwitch	0 = OSD display is disabled. 1 = OSD display is enabled.

***SCLKValue* (0x30)**	
SCLKValue	4-byte value that will set the **SCLKIRQ** ISR bit to 1 if the internal **SCLK** counter reaches this value.

***DiscType* (0x38)**		
15 - 2	**1**	**0**
reserved	SOSDelay	MajorType
Reserved bits must be 0.		
SOSDelay	0 = DVD-DSP device does not transmit the ID and IED bytes (first 6 bytes) of each DVD sector. Must be 0 if MajorType = 1 or if DVD-DSP interface is not used. 1 = DVD-DSP transmits ID and IED bytes of each DVD sector.	
MajorType	0 = DVD disc. Must be 0 if CodeSource = 1. 1 = CD disc.	

***BitstreamSelect* (0x40)**		
15 - 11	**10 - 1**	**0**
CBSelect	reserved	VidEntry

Reserved bits must be 0.

CBSelect	00000b = VideoCD and CD-I (FMV) sectors with embedded MPEG-1 system-multiplexed bitstream. 00010b = DVD video object (VOB) sectors. 00100b = CD-DA PCM stereo audio sectors. 00101b = VideoCD auxiliary sectors via DVD-DSP/CD-DSP interface to be stored in SDRAM after Mode 2 Form 1 sector block decoding. 00110b = DVD navigation file sectors (e.g. VTSI, VMGI) via DVD-DSP interface to be stored in SDRAM. 00111b = MPEG-1 system (ISO 11172-1,2,3) or MPEG-2 program (ISO 13818-1,2,3) stream. 01100b = MPEG-1 video (ISO 11172-2) or MPEG-2 video (ISO 13818-2) elementary stream. 01101b = MPEG-1 video (ISO 11172-2) or MPEG-1 audio (ISO 11172-3) elementary stream packetized (PES) according to ISO 11172-1. Also supported is MPEG-1 video (ISO 11172-2), MPEG-1 audio (ISO 11172-3), MPEG-2 video (ISO 13818-2) or MPEG-2 audio (ISO 13818-3) elementary stream packetized (PES) according to ISO 13818-1. Also supported is AC-3 audio, PCM audio, or sub-picture elementary stream packetized (PES) according to the DVD Specification 1.0. 01111b = MPEG-1 audio (ISO 11172-3) or MPEG-2 audio (ISO 13818-2) elementary stream. 10110b = AC-3 audio elementary stream. 11000b = LPCM audio elementary stream according to the DVD Specification 1.0. All other combinations are reserved and must not be used.
VidEntry	0 = Video entry point is 1st I-Picture header, GOP header or sequence header parsed in the bitstream. 1 = Video entry point it 1st sequence header parsed in the bitstream.

***PlaybackMode* (0x41)**							
15 - 10	**9**	**8, 7**	**6**	**5**	**4**	**3**	**2 - 0**
reserved	LastPic	reserved	VidFloat	reserved	Black	DVDReqEnable	reserved

Reserved bits must be 0.

LastPic	0 = Background color is displayed after decoding/displaying last video frame. 1 = Last frame is displayed after decoding/displaying last video frame.
VidFloat	0 = Pixel bus is tri-stated by VDEN# pin. This is the default after RESET. If changed from 1 to 0, a RESET must be applied. 1 = Entire video port is tri-stated. This overrides status of VDEN# and VMASTER input pins.
Black	0 = The programmed background color is displayed within the active area, outside the image area. 1 = While a decoded image is displayed in the image area, the active area outside the image area is black. When a decoded image is not displayed, this region switches to the programmed background color.
DVDReqEnable	0 = DVDREQ is enabled. This is normal operation. 1 = DVDREQ is disabled. This is a special operation mode for title key transfer during decryption as explained in a separate application note.

***AudSID* (0x42), *VidSID* (0x43), *SPSID* (0x44)**	
AudSID	8-bit stream ID or sub-stream ID (audio within Private 1 packets) for audio stream to be decoded. m.s. byte must be zero.
VidSID	8-bit stream ID for video stream to be decoded. m.s. byte must be zero.
SPSID	8-bit sub-stream ID for sub-picture stream to be decoded. m.s. byte must be zero.

***AudPortDelay* (0x45), *VidPortDelay* (0x46), *VidTolerance* (0x47)**	
AudPortDelay	Designates an additional delay to account for reconstruction chain delays. Measured in units of **SCLK** (90KHz). Used to synchronize audio and video. Must be 0 if no audio stream is decoded.
VidPortDelay	Designates an additional delay to account for reconstruction chain delays. Measured in units of **SCLK** (90KHz). Used to synchronize audio and video. Must be 0 if no video stream is decoded.
VidTolerance	Defines the tolerance allowed between the internal **SCLK** counter and the video frame's DTS to maintain synchronization. If this difference falls outside the tolerance, then a following video frame is either dropped (B-frames only) or the currently displayed frame is repeated. Measured in units of **SCLK** (90KHz). A value of 0 requires exact comparison. Must be 0 if no video stream is decoded.

***VidSyncMode* (0x48)**		
15 - 2	**1**	**0**
reserved	Vlock	VsyncMode
Reserved bits must be 0.		
Vlock	0 = no functionality. 1 = The transition of setting this bit from 0 to 1 causes **SCLK** to initialize to the next SCR in the bitstream. This can only be done between the **start** and **end_playback** host commands to take effect. This bit may remain 1 and have no effect. Once the bit is cleared, setting it again will cause the **SCLK** to reinitialize to the next SCR in the bitstream.	
VsyncMode	0 = Video does not synchronize to **SCLK** counter. 1 = Video synchronizes to **SCLK** counter.	

***SPPalette* (0x49)**	
SPPalette	16 x 32-bit sub-picture palette entries. Each 32-bit entry is in the format: Zeros[31:24] Y[23:16] V[15:8] U[7:0]. The sub-picture palette (PGC_SP_PLT) is typically extracted from the Program Chain Information (PGCI) on a DVD and is written to the **ZR36710** in the order it is found on the DVD.

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***AutoScaling* (0x50)**			
15	**14 - 3**	**2**	**1, 0**
DynPanEnable	reserved	VidFAR	VidFAC

Reserved bits must be 0.	
DynPanEnable	0 = **ZR36710** disables dynamic panning via DynPanX and DynPanY parameters. 1 = **ZR36710** enables dynamic panning via set-up parameters DynPanX and DynPanY parameters.
VidFAR	0 = Display frame aspect ratio is 4:3. Must be 0 if VidFAC = 00b. 1 = Display frame aspect ratio is 16:9.
VidFAC	00b = Display frame aspect ratio conversion (FAC) is handled by host. 01b = **ZR36710** performs automatic display FAC via horizontal scaling (e.g. Pan-scan). 10b = No display FAC, but will still calculate parameters for 1:1 scaling or NTSC/PAL conversion. 11b = **ZR36710** performs automatic display FAC via vertical scaling (e.g. Letterbox).

***PanScanBaseX* (0x51), *PanScanBaseY* (0x52), *PanScanSizeX* (0x53), *PanScanSizeY* (0x54), *PicSizeX* (0x55), *PicSizeY* (0x56)**	
PanScanBaseX	Defines the base number of decoded pixels at the beginning of each decoded line that are not displayed (skipped) before displaying the first decoded pixel of each decoded line. Minimum value is 0. Maximum value is (2 x int(HS/2) - 32) where HS is the horizontal size value extracted from the sequence header of the bitstream. The actual number of skipped decoded pixels at the beginning of each decoded line can be further changed by the PanScanOffsetX parameter (e.g. host handles Pan-scan) or by the frame_center_horizontal_offset value of the picture extension header (**ZR36710** handles Pan-scan automatically).
PanScanBaseY	Defines the base number of decoded lines at the beginning of each decoded field that are not displayed (skipped) before displaying the first decoded line of each decoded field. Minimum value is 0. Maximum value is (int(VS/2) - 16) for VS > 288 or (VS - 16) for VS <= 288 where VS is the vertical size value extracted from the sequence header of the bitstream. The actual number of skipped decoded lines at the beginning of each decoded field can further be changed by the PanScanOffsetY parameter (e.g. host handles vertical positioning) or by the frame_center_vertical_offset value of the picture extension header (**ZR36710** handles vertical positioning automatically).
PanScanSizeX	Defines the number of decoded pixels per decoded line that will be displayed. Minimum value is 32. Maximum value is (2 x int(HS/2) with HS as defined above. Must be a multiple of L_H.
PanScanSizeY	Defines the number of decoded lines per decoded field that will be displayed. Minimum value is 16. Maximum value is (int(VS/2) for VS > 288 or (VS) for VS < 288. Must be a multiple of L_V.
PicSizeX	If the number of decoded pixels per line > 384, PicSizeX = (PanScanSizeX - 1). If the number of decoded pixels per line <= 384, PicSizeX = (2 x PanScanSizeX - 1).
PicSizeY	PicSizeY = (PanScanSizeY - 1).

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***ImageStartX* (0x57), *ImageStartY* (0x58), *ImageSizeX* (0x59), *ImageSizeY* (0x5A), *ImageEndX* (0x5B), *ImageEndY* (0x5C)**	
ImageStartX	Number of background pixels at the beginning of each line prior to displaying the decoded picture, measured in the number of VCLKs after the effective edge of HSYNC. Must be even. Minimum value is (ActiveStartX). Maximum value is (ImageEndX - 16).
ImageStartY	Number of background lines at the beginning of each field prior to displaying the decoded picture, measured in the number of HSYNC pulses after the effective edge of VSYNC. Minimum value is (ActiveStartY). Maximum value is (ImageEndY - 16).
ImageSizeX	Number of decoded pixels to be displayed per line. Should be (ImageEndX - ImageStartX).
ImageSizeY	Number of decoded lines to be displayed per field. Should be (ImageEndY - ImageStartY).
ImageEndX	Indicates the number of pixels after the start of the line which decoded pixels are no longer displayed and background color is displayed, measured in the number of VCLKs after the effective edge of HSYNC. The number of background pixels displayed at the end of each line is (Htotal - ImageEndX). Must be even. Minimum value is (ImageStartX + 16). Maximum value is (ActiveEndX).
ImageEndY	Indicates the number of lines after the start of the field which decoded lines are no longer displayed and background color is displayed, measured in the number of HSYNC pulses after the effective edge of VSYNC. The number of background lines displayed at the end of each field is (int(Vtotal/2) - ImageEndY). Minimum value is (ImageStartY + 16). Maximum value is (ActiveEndY).

***ScaleRatio* (0x5E)**			
15 - 12	**11 - 8**	**7 - 4**	**3 - 0**
L_H	M_H	L_V	M_V
Host must write 0x0000 if **ZR36710** automatically scales the decoded video. These parameters are not used for fixed CCIR 601 scaling.			
L_H	Horizontal scaling ratio denominator. Minimum value is 1. Maximum value is 11.		
M_H	Horizontal scaling ration numerator. Minimum value is 1. Maximum value is 11. $3/4 <= M_H/L_H < 2$. $L_H = M_H = 1$ indicates bypass of horizontal scaling.		
L_V	Vertical scaling ratio denominator. Minimum value is 1. Maximum value is 11.		
M_V	Vertical scaling ratio numerator. Minimum value is 1. Maximum value is 11. $3/4 <= M_V/L_V < 2$. $L_V = M_V = 1$ indicates bypass of vertical scaling.		

***SPScale* (0x5F)**	
15 - 2	**1, 0**
reserved	SPvidstd
Reserved bits must be 0.	
SPvidstd	00b = No vertical scaling of sub-picture. 01b = Vertical scaling ratio is 5/6, scaling down PAL sub-picture for an NTSC display. 10b = Vertical scaling ratio of 6/5, scaling up NTSC sub-picture for PAL display. 11b = Reserved, do not use.

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***AutoPanScan* (0x68)**	
15 - 1	**0**
reserved	AutoPanScan
Reserved bits must be 0.	
AutoPanScan	0 = Host provides PanScan offset parameters. 1 = **ZR36710** automatically calculates PanScan offset parameters.

***PanScanOffsetX* (0x69), *PanScanOffsetY* (0x6A)**	
PanScanOffsetX	Additional offset number of decoded pixels skipped prior to display of decoded image. This value is a 16.4 twos-complement fraction. The two l.s. bits must be 0. If AutoPanScan = 0, the total offset of decoded pixels skipped per line is PanScanBaseX + PanScanOffsetX. This parameter is ignored if AutoPanScan = 1.
PanScanOffsetY	Additional offset number of decoded lines skipped prior to display of decoded image. This value is a 16.4 twos-complement fraction. The two l.s. bits must be 0. If AutoPanScan = 0, the total offset of decoded lines skipped per field is PanScanBaseY + PanScanOffsetY. This parameter is ignored if AutoPanScan = 1.

***BackgroundSwitch* (0x6B)**	
15 - 1	**0**
reserved	BackgroundSwitch
Reserved bits must be 0.	
BackgroundSwitch	0 = Decoded image and sub-picture is replaced with background color. OSD is not affected. 1 = Decoded image and sub-picture is displayed, if available.

***SPSwitch* (0x6C)**		
15 - 3	**2**	**1, 0**
reserved	SPSkip	SPDisplay
Reserved bits must be 0.		
SPSkip	0 = Reserved, do not use. 1 = Sub-pictures whose start time has already been passed by **SCLK** are displayed at least once.	
SPDisplay	00b = Reserved, do not use. 01b = Sub-picture is displayed on FSTA_DSP or STA_DSP sub-picture commands. 10b = Sub-picture is displayed on FSTA_DSP sub-picture commands only. 11b = Reserved, do not use.	

***CaptionWord* (0x6D)**	
CaptionWord	Data to be placed on closed caption line as closed caption data when playback is paused, if performing PAL to NTSC frame rate conversion or if CSwitch = 01b (used mostly for debugging). Host should initialize to 0x0000 prior to playback for proper operation of the closed caption modulator when playback is paused.

***CaptionSwitch* (0x6F)**	
15 - 2	**1, 0**
reserved	CSwitch
Reserved bits must be 0.	
CSwitch	00b = No data is output on closed caption line. 01b = Line 21 data is provided via CaptionWord parameter and displayed (used mostly for debugging). 10b = Line 21 data which is automatically extracted from GOP user data is displayed. 11b = Reserved, do not use.

***HiLightButton1* (0x70), *HiLightButton2* (0x71)**						
HiLightButton1	Coordinates (X start, X end, Y start, Y end: each 10 bits) and button color table (1 <= BTN_COLN <= 3, reflecting *HiLightColor1*, *HighLightColor2* or *HiLightColor3*, respectively) of HLI Button 1.					
	Bit 47	BTN_COLN	start X coord. (10 bits)	00b	end X coord. (2 m.s. bits)	Bit 32
	Bit 31	end X coord. (8 l.s. bits).	00b	start Y coord. (6 m.s. bits)		Bit 16
	Bit 15	start Y coord. (4 l.s. bits)	00b	end Y coord. (10 bits)		Bit 0
HiLightButton2	Coordinates of HLI Button 2 as defined above.					

***HiLightColor1* (0x72), *HiLightColor2* (0x75), *HiLightColor3* (0x76)**						
HiLightColor1	HLI palette indices and blending factors for four different color types for both “selected” and “activated” button states. Each palette index and blending factor is 4 bits. All 8 bytes must be entered, m.s. byte first as follows:					
	Bit 63	“selected” palette index for 11b color type.	“selected” palette index for 10b color type.	“selected” palette index for 01b color type.	“selected” palette index for 00b color type.	Bit 48
	Bit 47	“selected” blending factor for 11b type.	“selected” blending factor for 10b type.	“selected” blending factor for 01b type.	“selected” blending factor for 00b type.	Bit 32
	Bit 31	“activated” palette index for 11b type.	“activated” palette index for 10b type.	“activated” palette index for 01b type.	“activated” palette index for 00b type.	Bit 16
	Bit 15	“activated” blending factor for 11b type.	“activated” blending factor for 10b type.	“activated” blending factor for 01b type.	“activated” blending factor for 00b type.	Bit 0
HiLightColor2	Same definition as HiLightColor1 as defined above.					
HiLightColor3	Same definition as HiLightColor1 as defined above.					

***HiLightTiming* (0x73)**			
HiLightTiming	Timing values associated with the active button. The 12 bytes of this parameter are loaded m.s. byte first as follows:		
	Bit 95	HLI_S_PTM: Starting PTS of the hilight operation.	Bit 64
	Bit 63	HLI_E_PTM: Ending PTS of the hilight operation.	Bit 32
	Bit 31	BTN_SL_E_PTM: PTS at which button changes from “selected” to “activated” state.	Bit 0

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***HiLightSwitch* (0x74)**	
HiLightSwitch	0x0000 = Disable highlight function immediately (buttons return to current SPU color codes and blending factors). 0x0001 = Hilight Button 1 using the “selected” set, starting at HLI_S_PTM until BTN_SL_E_PTM. Then hilight Button 1 using the “activated” set until HLI_E_PTM, then disable hilighting. 0x0002 = Hilight Button 1 using the “selected” set, starting immediately (only if HLI_S_PTM has been passed by **SCLK**) until BTN_SL_E_PTM. Then hilight Button 1 using the “activated” set until HLI_E_PTM, then disable hilighting. 0x0003 = Hilight Button 1 using the “selected” set, starting at HLI_S_PTM until BTN_SL_E_PTM. Then hilight Button 2 using the “activated” set until HLI_E_PTM, then disable hilighting. 0x0004 = Hilight Button 1 using the “selected” set, starting immediately (only if HLI_S_PTM has been passed by **SCLK**) until BTN_SL_E_PTM. Then hilight Button 2 using the “activated” set until HLI_E_PTM, then disable hilighting. 0x0005 = Hilight Button 1 using the “selected” set, starting at HLI_S_PTM until HLI_E_PTM, then disable hilighting. 0x0006 = Hilight Button 1 using the “selected” set, starting immediately (only if HLI_S_PTM has been passed by **SCLK**) until HLI_E_PTM, then disable hilighting. 0x0007 = Hilight Button 1 using the “activated” set, starting immediately (only if HLI_S_PTM has been passed by **SCLK**) until HLI_E_PTM (or a stop indication). 0x0008 = Hilight Button 2 using the “activated” set, starting immediately (only if HLI_S_PTM has been passed by **SCLK**) until HLI_E_PTM (or a stop indication). 0x0009 - 0xFFFF are reserved and should not be used.

***OSDPalette0i* (0x80 - 0x8F), *OSDPalette1i* (0x90 - 0x9F)**				
31 - 26	**25,24**	**23 - 16**	**15 - 8**	**7 - 0**
reserved	OSDBF	8-bit Y component	8-bit U component	8-bit V component
Reserved bits must be 0.				
OSDBF	00b = Blending ratio is 0% OSD and 100% video/sub-picture/background. OSD display is disabled. 01b = Blending ratio is 25% OSD and 75% video/sub-picture/background. 10b = Blending ratio is 50% OSD and 50% video/sub-picture/background. 11b = Blending ratio is 100% OSD and 0% video/sub-picture/background. OSD is always “on top”.			

***DVPCmd* (0xCE)**	
DVPCmd	This parameter is used to write special host commands to the DVP for various functions such as reverse playback of DVD bitstreams. Refer to the microcode release notes for further details.

***DecCntr* (0xCF)**	
DecCntr	After the host no longer needs a NAV segment, 0x00 must be written to this parameter. Only needed if the **ZR36710** will stop requesting bitstream if the NAV segments are not read quickly enough.

***DynPanX* (0xE0), *DynPantY* (0xE1)**	
DynPanX	Additional offset number of decoded pixels skipped prior to display of decoded image for the purpose of dynamic panning (even while the decoded image is paused). This value is a 16.2 unsigned fraction. If DynPanEnable = 1, the total offset of decoded pixels skipped per line is PanScanBaseX + DynPanX. This parameter is ignored if DynPanEnable = 0.
DynPanY	Additional offset number of decoded lines skipped prior to display of decoded image for the purpose of dynamic panning (even while the decoded image is paused). This value is a 16.2 unsigned fraction. If DynPanEnable = 1, the total offset of decoded lines skipped per field is PanScanBaseY + DynPanY. This parameter is ignored if DynPanEnable = 0.

5.1.3 Loading Microcode via the General Set-up Parameters

Zoran provides various microcode and initialization files that are to be loaded into the **ZR36710** in order for the device to carry out its various playback functions. These microcode and initialization files are accompanied by release notes that explain what files are provided and under which circumstances each file needs to be loaded to the device. The **ZR36710** requires microcode and initialization files to be loaded via the following indexed addresses of the general set-up parameter address space:

- 0xFD: DVP microcode.
- 0xF0: Initialization (Init) file #1.
- 0xF1: Init file #2.
- 0xF2: Init file #3.
- 0xF3: Init file #4.

Init file #3 can be loaded only once after each time the **ZR36710** is taken out of RESET.

As an indication that the DVP microcode has been successfully loaded, the **ZR36710** has a simple authentication routine. Immediately after receiving the first **start**[1] host command, the device writes the 8-bit microcode revision number to the **DVPGPFL[7:0]** bits in the **STATUS2**[2] register. The host may read and verify this value.

If the host loads a DVP microcode and then needs to load a different DVP microcode prior to issuing a **start** host command, then the host needs to zero-pad the original DVP microcode to 16384 bytes before loading the replacement microcode.

The DVP microcode is required by the DVP to properly decode the various supported bitstreams. An application such as a DVD player may load different DVP microcode when switching between types of bitstreams (e.g. changing from a DVD to a VideoCD). The microcode release notes specify at which initialization stage each file can be loaded.

1. See Section 6.11 “Host Commands and Control over the Playback Operation” for an explanation of writing host commands to the **ZR36710**.
2. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

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5.2 Interrupt Status and Mask Registers, Reg. 0x2

The **ZR36710** has a single interrupt request output, ***HIRQ#***. This active-low signal, described in Section 4.3.4 “Interrupt Signal - HIRQ#”, can be activated by any one or more of several possible interrupting events that occur within the device. The host can query the device to see which particular event(s) caused the interrupt by reading register 0x2, the Interrupt Status Register (ISR). Reading the ISR will also de-assert the ***HIRQ#*** pin until another interrupt event occurs, re-asserting the pin. The host can mask which events can and cannot cause interrupts by writing the appropriate value to register 0x2, the Interrupt Mask Register (IMR).

TABLE 35. ZR36710 Interrupt Status and Mask Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

Each event is represented by a flag bit in the Interrupt Status Register (ISR), and a corresponding mask bit in the Interrupt Mask Register (IMR). On an interrupt event, the following occurs:

- The bit in the ISR corresponding to the event that occurred is set to 1.
- If the corresponding bit in the IMR is equal to 0, the ***HIRQ#*** output of the **ZR36710** is asserted low.
- The ***HIRQ#*** output remains asserted until the host reads the ISR.

The asserted ISR bit(s) remain equal to 1 until the event that clears it (them) happens (in some cases this is the host reading of the ISR, but not in all cases). As implied by the above sequence of events, bits in the ISR will be set by certain events, but this does not mean that interrupts are triggered unless the corresponding bits in the IMR are cleared.

The interrupting triggering events are listed below according to the order of their corresponding bits in the ISR and IMR, from bit 15 down to 0. The values of the reserved bits are not guaranteed, so they must be masked out and ignored when read.

Interrupt Status Register (ISR - Read Register 0x2) and Interrupt Mask Register (IMR - Write Register 0x02)												
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3 - 0**
NAVREADY	DVPOBF	VSYNC	PLLpLOCKED	PLLaLOCKED	res.	DVPSWIRQ	ADPSWIRQ	res.	SCLKIRQ	res.	CODBUFIRQ	res.

res. = Reserved, value must be ignored by system since value on ISR bit is undefined.

NAVREADY	NAV Data Ready. This bit is set when a new navigation pack (NV_PCK as described in the DVD Specification 1.0) is extracted from the bitstream and stored in the SDRAM. See Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”. Up to eight NV_PCKs can be stored in SDRAM and three bits of the **STATUS1** register (see Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)”) indicate which NV_PCK to read on this interrupt. This bit is cleared automatically when the ISR is read.
DVPOBF	Demultiplexer/Video Processor (DVP) Output Buffer Full. This bit is set when the DVP Output FIFO is full (64 words). On this interrupt, the host should read the entire 64 words via the DVP Output Data Register (0x6). See Section 5.6.2 “Reading Data from the DVP Data Register”. This bit is cleared whenever there is less than 64 words in this FIFO (when the FIFO is not full).
VSYNC	Vertical Sync. This bit is set with every effective edge of ***VSYNC*** as selected by the *VEdge*[a] parameter. This bit is cleared automatically when the ISR is read.
PLLpLOCKED	***PCLK*** Stable. This bit is set whenever ***PCLK*** is locked. See Section 4.2 “Phase-Locked Loop Interface”. This bit is cleared whenever ***PCLK*** is not locked by the PLL circuit.
PLLaLOCKED	***AMCLK*** Stable. This bit is set whenever ***AMCLK*** is locked. See Section 4.2 “Phase-Locked Loop Interface”. This bit is cleared whenever ***AMCLK*** is not locked by the PLL circuit.
DVPSWIRQ	DVP Software Flag. This bit is set to 1 by the DVP microcode. Microcode release notes will explain the functionality of this flag as it pertains to each version of DVP microcode. This bit is cleared automatically when the ISR is read.
ADPSWIRQ	ADP Software Flag. This bit is set to 1 by the ADP microcode. Microcode release notes will explain the functionality of this flag as it pertains to each version of ADP microcode. This bit is cleared automatically when the ISR is read.
SCLKIRQ	*SCLKValue* Interrupt. This bit is set to 1 once the internal **SCLK** counter has passed the value written to the *SCLKValue*[a] set-up parameter. See Section 6.10.1 “Internal SCLK Counter”. This bit is cleared automatically when the ISR is read.
CODBUFIRQ	Code Buffer Over/Underflow. This bit is set to 1 for one of the following events (see Section 6.5 “Stream Demultiplexing”): 1. Overflow in either the video code buffer, audio code buffer or sub-picture code buffer. 2. Underflow in either the video code buffer or audio code buffer. This bit is cleared automatically when the ISR is read.

a. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

After RESET, the IMR has an internal default value of 0xFFFF, disabling all interrupts to the host.

5.3 Issuing Host Commands - Reg. 0x3 (Write)

Host commands are written to the Host Command Register. All host commands consist of a 16-bit word. Before writing a host command, the host must check that the **HCREADY** bit in the **STATUS1**[1] register is equal to 1.

TABLE 36. ZR36710 Host Command Register

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

The different host commands are detailed in Section 6.11 “Host Commands and Control over the Playback Operation”.

5.4 Host Interface for Coded Bitstream - Reg. 0x4 (Write)

If the **ZR36710** does not receive coded bitstream via the DVD-DSP (or CD-DSP) interface, then it must receive the bitstream through write register 0x4, the Coded Bitstream Register. The *CodeSource* bit of the *SysConfig*[2] set-up parameter must be set to 1. The protocol between the host and the **ZR36710** for coded bitstream transfers is explained in Section 4.3.5 “Coded Data Request for Host Bus Code Transfers - HRDY”.

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.
2. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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TABLE 37. ZR36710 Coded Bitstream Register

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

The ***HRDY*** output pin and **HRDY** bit of the **STATUS1**[1] register indicate to the host if the **ZR36710** can be accessed with coded bitstream. A high level on either signal indicates that up to *CodBurstLen*[2] code bytes can be written without having to check ***HRDY*** again. *CodBurstLen* is a 8-bit parameter that can get the following values: 4, 8, 16, 32 or 64. The **ZR36710** host interface includes an internal 64-byte FIFO dedicated for bitstream input.

After ***HRDY*** is de-asserted, a number of code bytes may be further written to the **ZR36710**, such that the total number of bytes, written since the last time ***HRDY*** was high, will be *CodBurstLen.*

If the host does not monitor the status of the code FIFO via the ***HRDY*** pin or **HRDY** status bit, then the host risks overwriting unread data within the FIFO, causing bitstream errors. There is an alternative to this rule with regards to the ***HACK#*** signal as explained in Section 4.3.5 “Coded Data Request for Host Bus Code Transfers - HRDY”.

As explained in Section 4.3.3 “Address/Register Space and Register Access”, writes to the Coded Bitstream Register can interrupt transfers to other registers. For example, if 64 bytes are in the process of being written to the Parameter Data Register, writes to the Coded Bitstream Register can interrupt this process at any time.

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.
2. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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5.5 Status Registers - Reg. 0x3, 0x4, 0x5 (Read)

The **ZR36710** has three 16-bit status registers, **STATUS0** (read register 0x3), **STATUS1** (read register 0x4) and **STATUS2** (read register 0x5). These registers contain status information for various aspects of the **ZR36710**. These registers can be read at any time to inform the system of the current status of the device.

TABLE 38. ZR36710 Status Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

Unless otherwise specified, reading status data does not affect the data (unlike reading the ISR which clears several bits). The information indicated by each of the bits and the timing of setting these bits to 1 and clearing these bits is described in the following tables. The values of the reserved bits are not guaranteed, so they should be ignored when read.

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STATUS0 Register (Read Register 0x3)										
15 - 10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C-STATE	reserved	DRAMBE	DRAMBF	VCBE	VCBF	ACBE	ACBF	SPCBF	ADPEMPTY	ADPRDY

Reserved bit values must be ignored by system since value is undefined.	
C-STATE	Internal operating state. Several of these states are reflective of the last host command issued to the device as explained in Section 6.11 “Host Commands and Control over the Playback Operation”. Allowed values are as follows: 00 0000b = ***reset*** state: The period between RESET and locking of ***PCLK*** by the PLL circuitry. 00 0010b = ***init_pclk*** state: The period while ***PCLK*** is locked, but the *StartDisplay*[a] parameter has not been given. 00 0011b = ***init_display***: The period after *StartDisplay* has been given, but prior to a **start** host command. 01 0000b = ***Pause*** (active video) state: Playback is paused with the output of a frame. 01 1000b = ***Pause*** (no active video) state: Playback is paused with no decoding/display of a frame. 10 0000b = ***Nspb*** (active video) state: Non-stop playback with the output of a frame. 10 1000b = ***Nspb*** (no active video) state: Non-stop playback with no decoding/display of a frame. 10 0011b = ***Step*** (active video) state: Single-step playback. 10 1011b = ***Step*** (no active video) state: Single-step playback. 10 0101b = ***Slow*** (active video) state: Slow-motion playback. 10 1101b = ***Slow*** (no active video) state: Slow-motion playback. 11 0000b = ***Idle*** state: Period between end of decoding and next **start** host command. All other combinations are reserved and must not be used.
DRAMBE	0 = DRAM 32-word FIFO (for OSD data transfers) is not empty. See Section 5.11 “Writing OSD Data - Reg. 0xB and 0xC (Write)”. 1 = DRAM 32-word FIFO (for OSD data transfers) is empty. Host may write up to 32 words to the OSD register before checking this bit again.
DRAMBF	0 = DRAM 32-word FIFO (for NV_PCK transfers) is not full. See Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”. 1 = DRAM 32-word FIFO (for NV_PCK transfers) is full. Host may read 32 words from the NAV data register before checking this bit again.
VCBE	0 = Video code buffer in SDRAM is not empty. See Section 6.5 “Stream Demultiplexing”. 1 = Video code buffer in SDRAM is empty. Once set to 1, this bit remains 1 until cleared by a read to this status register, no matter if data became present in the buffer after this bit was set to 1.
VCBF	0 = Video code buffer in SDRAM is not full. See Section 6.5 “Stream Demultiplexing”. 1 = Video code buffer in SDRAM is full. Once set to 1, this bit remains 1 until cleared by a read to this status register, no matter if data was flushed from the buffer after this bit was set to 1.
ACBE	0 = Audio code buffer in SDRAM is not empty. See Section 6.5 “Stream Demultiplexing”. 1 = Audio code buffer in SDRAM is empty. Once set to 1, this bit remains 1 until cleared by a read to this status register, no matter if data became present in the buffer after this bit was set to 1.
ACBF	0 = Audio code buffer in SDRAM is not full. See Section 6.5 “Stream Demultiplexing”. 1 = Audio code buffer in SDRAM is full. Once set to 1, this bit remains 1 until cleared by a read to this status register, no matter if data became present in the buffer after this bit was set to 1.
SPCBF	0 = Sub-picture code buffer in SDRAM is not full. See Section 6.5 “Stream Demultiplexing”. 1 = Sub-picture code buffer in SDRAM is full. Once set to 1, this bit remains 1 until cleared by a read to this status register, no matter if data became present in the buffer after this bit was set to 1.
ADPEMPTY	0 = ADP Data Register is not ready to receive a byte from the host. See Section 5.8 “ADP Access - Reg. 0x8”. 1 = ADP Data Register is ready to receive a byte from the host.
ADPRDY	0 = ADP Status Register does not contain a valid byte for the host to read. See Section 5.8 “ADP Access - Reg. 0x8”. 1 = ADP Status Register contains a valid byte for the host to read.

a. See Section 5.1 “General Set-up Parameters and Microcode - Reg. 0x0 and 0x1” for an explanation on loading set-up parameters to the **ZR36710**.

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STATUS1 Register (Read Register 0x4)											
15	**14**	**13, 12**	**11**	**10**	**9**	**8**	**7**	**6, 5**	**4, 3**	**2**	**1, 0**
HCREADY	STARVING	PICTYPE	HRDY	IDLE	FRAME/FIELD#	DVPVAL	DVPIBE	NAVBUF	HLI_TIME	SPDERR	DVP_SW[1:0]

HCREADY	0 = **ZR36710** is not ready to receive host command via Host Command Register. See Section 6.11 “Host Commands and Control over the Playback Operation”. 1 = **ZR36710** is ready to receive host command.
STARVING	0 = Normal operation. 1 = Video decoding is paused automatically due to video buffer starvation or if during synchronized playback, **SCLK** is less than the next frame’s DTS (including *VidTolerance*). Cleared when video decoding resumes.
PICTYPE	00b = No MPEG picture is currently being decoded. 01b = I-picture is currently being decoded. 10b = P-picture is currently being decoded. 11b = B-picture is currently being decoded. Set on ***VSYNC*** immediately after decoding of first block. Reset to 00b on next ***VSYNC*** unless it is an MPEG-2 field picture. See Section 6.6 “Video Decoding”.
HRDY	0 = ***HRDY*** pin is low. Used to accommodate systems that do not poll the ***HRDY*** pin. 1 = ***HRDY*** pin is high. See Section 4.3.5 “Coded Data Request for Host Bus Code Transfers - HRDY”.
IDLE	0 = ***IDLE*** pin is low. Used to accommodate systems that do not poll the ***IDLE*** pin. 1 = ***IDLE*** pin is high. See Section 14.3 “Stage 3: OSD Display and Preparation for Decoding”.
FRAME/FIELD#	0 = Picture being decoded is an MPEG-2 field picture. 1 = Picture being decoded is an MPEG-1 or MPEG-2 frame picture. See Section 6.6 “Video Decoding”.
DVPVAL	0 = Data read from the DVP Data Register is valid. 1 = Data read from the DVP Data Register is invalid. This bit is cleared by a read from this status register. See Section 5.6.2 “Reading Data from the DVP Data Register”.
DVPIBE	0 = DVP input FIFO associated with the DVP Data Register is not empty. 1 = DVP input FIFO associated with the DVP Data Register is empty. Host may write up to 64 bytes to the DVP Data Register before checking this bit again. Bit is cleared once the 64th byte is written to this register. See Section 5.6.1 “Writing Data to the DVP Data Register”.
NAVBUF	The two l.s. bits of the 3-bit NAV segment counter (DVP_SW[0] is the m.s. bit) used to indicate which NAV buffer segment has most recently had NV_PCK information copied to. 11b is the default value after RESET. See Section 5.10 “Reading the NAV Buffer in SDRAM - Reg. 0xA”.
HLI_TIME	00b = HLI is disabled. Default value after RESET. 01b = **SCLK** counter falls within the selection period of an HLI. 10b = **SCLK** counter falls within the activation period of an HLI. 11b = **SCLK** counter falls after the activation period of an HLI. See Section 6.8.4 “Highlight Parameters”.
SPDERR	0 = No error within the internal sub-picture decoder. See Section 6.8 “Sub-Picture Decoding with HLI Support”. 1 = An internal sub-picture decoder error occurred since the last time this status register was read. This bit is cleared when this status register is read.
DVP_SW[1:0]	Generic status flags used by the DVP for various functions. One of DVP_SW[0]’s functions is as the m.s. bit (along with NAVBUF) of a 3-bit NAV segment counter used to indicate which NAV buffer segment has most recently had NV_PCK information copied to. For other functions, refer to microcode release notes for details.

STATUS2 Register (Read Register 0x5)	
15 - 8	**7 - 0**
DVPGPFL[7:0]	reserved
Reserved bit values must be ignored by system since value is undefined.	
DVPGPFL[7:0]	DVP General Purpose Flags. These bits are set and cleared by the DVP microcode. As explained in this document, these bits have various functionality depending on the task of the DVP. Currently defined functionality includes: 1. Indication of the DVP microcode version as explained in Section 5.1.3 “Loading Microcode via the General Set-up Parameters”. 2. Bitstream error indication as explained in Section 6.9 “Error Indication and Concealment”. 3. Indication of how many DVD auxiliary sectors are stored in the SDRAM as explained in Section 14.11 “Also For: DVD Navigation File Sectors”. Refer to the microcode release notes for changes/additions in the functionality of these bits.

5.6 Writing and Reading the DVP Data Register - Reg. 0x6

The **ZR36710** allows data transfer between the host and DVP through the DVP Data Register. Writes to this register are queued in an input FIFO and retrieved by the DVP as instructed by the DVP microcode. When the DVP wants the host to retrieve data, it queues the data in an output FIFO and informs the host (as explained in the following sub-sections) that data is ready for the host to read.

TABLE 39. ZR36710 DVP Data Register

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

5.6.1 Writing Data to the DVP Data Register

The protocol of writing to the DVP Data Register is shown in Table 40 :

TABLE 40. Protocol of Writing to the DVP Data Register

Protocol
Step 1: The host reads the **STATUS1**[a] register, checking for **DVPIBE** = 1.
Step 2: If **DVPIBE** = 1, the host writes 64 bytes (32 words) to the DVP Data Register, loading the data into a FIFO that will be read by the DVP.

a. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

Upon writing the last byte (or word), the **ZR36710** will clear the **DVPIBE** bit which indicates to the DVP that the FIFO is full and data may be read. If less than 64 bytes are written to this register, the **DVPIBE** bit will not be cleared and the DVP will not read the data from the FIFO so 64 bytes must be written.

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Data Format Written to the DVP Input FIFO

The following shows the data format that is written to the DVP Input FIFO.

TABLE 41. Data Format Written to the DVP Input FIFO

Input Order of Each 16-bit DVP Input FIFO Entry
Type
parameter 1
...
parameter 31

Data Types Provided to the DVP by the Host

Currently defined are two types of data the host provides to the DVP. Each of these types is uniquely identified by the first word written to the DVP Input FIFO (“Type” as shown in Table 41). Refer to the microcode release notes if these definitions have changed:

- No data (Type = 0x0000). Parameters 1 - 31 must be written, but contain no valid data.
- Start and end sector addresses for VideoCD playback via the CD-DSP interface. The details of VideoCD playback via this interface are given in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”.

5.6.2 Reading Data from the DVP Data Register

The DVP parses bitstream data, extracts certain data and provides this extracted data to the host for further processing. This data is queued in a 64-word DVP output FIFO, denoted DVPO_FIFO. The protocol for data retrieval from the DVPO_FIFO via the DVP Data Register is shown in Table 42 . This protocol is explained further in Section 14.4 “Decoding/Playback”:

TABLE 42. Protocol of Reading Data from the DVP Data Register

Protocol
Step 1: The **ZR36710** sets the **DVPOBF** bit in the ISR[a] to 1 once the DVPO_FIFO has been filled by the DVP. If the IMR enables this event to trigger an interrupt, then the host receives an interrupt.
Step 2: If **DVPOBF** = 1, the host reads 64 words from the DVP Data Register. The **DVPOBF** bit is cleared once the first word is read from the DVPO_FIFO.
Step 3: After reading the data, the host reads the **STATUS1**[b] register, checking for **DVPVAL** = 0.
Step 4: If **DVPVAL** = 0, the data read was valid. If **DVPVAL** = 1, the data was overwritten by the DVP with new data while being read and should be discarded by the host.
To avoid data being invalidated by the DVP, the following protocol is recommended:
Step 1: On each ***VSYNC*** interrupt, the **DVPOBF** bit is checked. The **DVPOBF** bit is masked in the IMR to not trigger interrupts.
Step 2: If **DVPOBF** = 1, the host reads 64 words from the DVP Data Register.
Step 3: The host checks for **DVPVAL** = 0 to validate the data. Reading data (if there is data to read) on every ***VSYNC*** should avoid data within the DVPO_FIFO to be overwritten.

a. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.

b. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

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DVP Data Types Provided to the Host

Currently defined are seven types of data that the DVP provides to the host as shown below. Refer to the microcode release notes if the definitions of these types of data has changed from what's shown here:

- VideoCD user data (closed captions and pointers to I-pictures). This data type is applicable only in playback of VideoCD discs.
- DVD closed captions user data. Applicable only in playback of DVD discs.
- Sequence header and sequence display extension video parameters. This data type consists of video parameters extracted from the MPEG-1/MPEG-2 sequence header that are provided to the host for possible parameter processing.
- Picture header, picture display extension and picture copyright extension video and copyright parameters. This data type consists of parameters extracted from the MPEG-1/MPEG-2 picture header and extensions that are provided to the host for possible parameter processing.
- A PAUSE_DRIVE request. This data type is applicable only in playback of VideoCDs via the CD-DSP interface and is explained in Section 14.6 "Also For: VideoCD or CD-I (FMV) Streams".
- A RESUME_DRIVE request. This data type is applicable only in playback of VideoCDs via the CD-DSP interface and is explained in Section 14.6 "Also For: VideoCD or CD-I (FMV) Streams".
- A GLOBAL_DELTA value used in handling SCR discontinuities in DVD bitstreams as explained in Section 6.10.5 "Handling SCR Discontinuities".

Either of the first two data types (but not both) and the third and fourth data types can all coexist within the DVPO_FIFO at the same time. In such a case they are ordered in sequential segments (each segment is a different data type) as explained in the following section.

5.6.2.1 Data Format in the DVPO_FIFO

Each data type segment in the DVPO_FIFO is preceded by a 16-bit designator called DVP Data Tag. It indicates the type and size of the data segment immediately following the Tag as shown in Table 43 .

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TABLE 43. 16-bit DVP Data Tag Format

Bit Assignment		
15, 14	**13 - 7**	**6 - 0**
Data Type	Number of Data Words in the Segment	Type-Dependent Information
Data Type	00b = VideoCD user data or DVD GOP header user data for closed captions. 01b = Sequence header parameters, a PAUSE_DRIVE request during VideoCD playback, a RESUME_DRIVE request during VideoCD playback or a GLOBAL_DELTA value used in handling SCR discontinuities as specified by bits 6:0. 10b = Picture header parameters. 11b = No data segment in the rest of the DVPO_FIFO. This indicates to the host that the rest of the buffer does not include any valuable data.	
Number of Words	Specifies the number of (16-bit) words in the data segment, excluding the Tag itself.	
Type-Dependent Information	For DVD GOP header closed captions data, these bits are defined as: Bit 6: “top_field_flag_of_gop” parameter. Bits 5:0: “number_of_displayed_field_gop” parameter. To determine if the data type 01b indicates sequence header parameters, a PAUSE_DRIVE request, a RESUME_DRIVE request or a GLOBAL_DELTA: Bits 6:0: 000 0000b - Sequence header parameters Bits 6:0: 000 0001b - PAUSE_DRIVE request as explained in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”. Bits 6:0: 000 0010b - RESUME_DRIVE request as explained in Section 14.6 “Also For: VideoCD or CD-I (FMV) Streams”. Bits 6:0: 000 0101b - GLOBAL_DELTA as explained in Section 6.10.5 “Handling SCR Discontinuities”. For other types of data segments: Bits 6:0 are all zeros.	

The format of the PAUSE_DRIVE, RESUME_DRIVE and GLOBAL_DELTA data segments are given in their respective sections referenced in Table 43 . The format for each of the other data segments is described in Table 44 .

TABLE 44. Format of DVPO_FIFO Data Within Each Segment

Type	Format
Picture User Data in MPEG-1 Video Streams	The number of words is always 32. The DVP may either truncate or zero-pad the original data to fit into the 32-word limit.
GOP User Data (Closed Captions in MPEG-2 Video Streams from DVD	The number of data words in this Tag is 39. If the number of displayed fields, n, is less than or equal to 16, the first n words after the Tag are captions words, in order. The next word is composed of the n l21_switch bits, in order, starting with the m.s. bit. The 16-n l.s. bits are set to 0. The last 35-n data words are written with 0xFFFF. If the number of displayed fields, n, is less than or equal to 32, the first 16 words after the Tag are captions words, in order. The next word is composed of the 16 first l21_switch bits, in order, starting with the m.s. bit. The next n-16 words are the last captions words, in order. The next word is composed of the last n-16 l21_switch bits, in order, starting with the m.s. bit. The 32-n l.s. bits are set to 0. The last 34-n data words are written with 0xFFFF. If the number of displayed fields, n, is more than 32, the first 16 words after the Tag are captions words, in order. The next word is composed of the 16 first l21_switch bits, in order, starting with the m.s. bit. The next 16 words are the next captions words, in order. The next word is composed of the second set of 16 l21_switch bits, in order, starting with the m.s. bit. The next n-32 words are the last captions words, in order. The next word is composed of the last n-32 l21_switch bits in order starting with the m.s. bit. The 48-n l.s. bits are set to 0. the last 34-n data words are written with 0xFFFF.
Sequence Parameters in MPEG-1 and MPEG-2 Video Streams	The number of data words in this Tag is 5. The DVP extracts the parameters listed below from the video stream and writes them to the buffer, if they exist in the bitstream. Note that in MPEG-1 the extension parameters do not exist. For each non-existent parameter, the word 0xFFFF is written. **1st word**: 4 leading zeros followed by horizontal_size_value (12 bits) for MPEG-2, or horizontal_size (12 bits) for MPEG-1. **2nd word**: 4 leading zeros followed by vertical_size_value (12 bits) for MPEG-2, or vertical_size (12 bits) for MPEG-1. **3rd word**: aspect_ratio_information (4 bits) for MPEG-2, or pel_aspect_ratio (4 bits) for MPEG-1, followed by frame_rate_code (4 bits) for MPEG-2, or picture_rate (4 bits) for MPEG-1, followed by 7 zeros, followed by progressive_sequence (1 bit) for MPEG-2 or a zero bit for MPEG-1. **4th word**: 2 leading zeros followed by display_horizontal_size (14 bits) for MPEG-2. **5th word**: 2 leading zeros followed by display_vertical_size (14 bits) for MPEG-2.
Picture Parameters in MPEG-2 Video Streams	The number of data words in this Tag is 13. The DVP extracts the parameters listed below from the video stream and writes them to the buffer, if they exist in the bitstream. Note that the 'offset' parameters appear for each field in the picture, so they may appear three times (in case of a frame picture with repeat_first_field). For each non-existent parameter, the word 0xFFFF is written. **1st word**: 2 leading zeros, followed by picture_structure (bits 13,12), followed by top_field_first (bit 11), followed by 5 zeros, followed by repeat_first_field (bit 5), followed by 1 zero, followed by progressive_frame (bit 3), followed by 3 zeros. **2nd word**: first frame_center_horizontal_offset (16 bits). **3rd word**: first frame_center_vertical_offset (16 bits). **4th word**: second frame_center_horizontal_offset (16 bits). **5th word**: second frame_center_vertical_offset (16 bits). **6th word**: third frame_center_horizontal_offset (16 bits). **7th word**: third frame_center_vertical_offset (16 bits). **8th to 13th word**: copyright extension data (first word first), if it exists.

5.6.2.2 How the DVP Fills the DVPO_FIFO

The DVP initiates writing of sequence header parameter data if it recognizes a “new” sequence header. A new sequence header is defined as the first sequence header immediately following an end_of_sequence marker or the first sequence header after a **start**[1] host command. The DVP writes the parameters according to the format described above.

Next, the DVP initiates writing the user data for line 21 if it encounters such data in the GOP header. For GOP headers that do not immediately follow a sequence header, the GOP user data is written starting from the beginning of the buffer. If a picture header appears in the bitstream before a GOP header is encountered, then no GOP header data is written at this time.

Next, the DVP initiates writing of the picture header parameters if it encounters a picture header. A picture header can appear after a GOP header, after a sequence header or with no other header prior to it. In any case, the picture header parameters are written starting from the upper most available address in the buffer - it may be the beginning of the buffer, just after the sequence header data segment or just after the GOP header data segment. The picture header data segment is immediately followed by a “no more data” Tag (2-bit Tag followed by 14 zeros).

Only after writing the “no more data” Tag into the buffer does the DVP raise the **DVPOBF** bit.

1. See Section 6.11 “Host Commands and Control over the Playback Operation” for an explanation on writing host commands to the **ZR36710**.

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5.7 Device ID Register - Reg. 0x7 (Read)

This register contains a hardwired value that represents the device ID and revision number.

TABLE 45. ZR36710 Device ID Register

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

The 8 m.s. bits are the device ID: 0x34.

The 8 l.s. bits are the revision number: 0xC0 for the first revision, 0xC1 for the second, etc.

5.8 ADP Access - Reg. 0x8

Access to the **ZR36710**'s Audio Data Processor (ADP) is done through two registers. Writes to the ADP that include ADP microcode downloading and issuing ADP commands are done via writes to register 0x8, the ADP Data Register. Various status bits that are returned after each byte is written to the ADP can be checked via reads from register 0x8, the ADP Status Register.

Writes to the ADP Data Register use only the 8 l.s. bits of the host bus interface. If a 16-bit host data bus is used, the 8 m.s. bits are ignored by the device. If an 8-bit host data bus is used, a byte of 0x00 must be written prior to each byte written of actual ADP data.

TABLE 46. ZR36710 ADP Status and Data Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

ADP Write Protocol - ADP Command Format

The protocol of writing data to the ADP conforms to the ADP command format explained in its entirety in Section 12. “Annex A: ADP Commands”. All data, including ADP microcode and ADP configuration parameters, is written as part of a particular ADP command.

To ascertain that the ADP is ready to accept a byte, a status bit **(ADPEMPTY)** in the **STATUS0**[1] register is provided. This status bit should be verified high by the host before writing a byte to the ADP Data Register.

5.8.1 ADP Configuration Commands

Section 5.1.2 “General Set-up Parameter List” provides a list of the general set-up parameters that the **ZR36710** requires to have initialized for proper operation of the device. In addition, the ADP also requires several ADP commands to be executed in order to initialize the ADP for proper operation as explained in Section 12. “Annex A: ADP Commands”. These ADP commands are listed in Table 47 .

1. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

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TABLE 47. ADP Configuration Commands

ADP Commands	Description	Initialization stage
PLLTAB, PLLCFG	***PCLK*** and ***AMCLK*** configuration.	***PCLK*****: C-STATE** = ***init_pclk*** ***AMCLK***: **C-STATE** = ***init_pclk*** with option to change during playback.
CFG, SPDIFCS	Audio port configuration	**C-STATE** = ***init_pclk***
PARAM (EXT = 0x00)	Audio output gain	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
MUTE, UNMUTE	Switch Audio mute on and off	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
PARAM (EXT = 0x02)	Audio synchronization tolerance (**SCLK** units)	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
PARAM (EXT = 0x03)	Audio synchronization mode selection	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***, with option to change during playback
BOOT	ADP microcode	**C-STATE** = ***init_display*** or **C-STATE** = ***Idle***

5.8.2 Writing ADP Microcode

Microcode is loaded to the ADP via the BOOT[1] ADP command into an on-chip ADP program RAM. The maximum size of the ADP microcode can be 12288 bytes. The host may load a smaller program (or not load any ADP microcode), but such a program must assure that the unloaded portion of the program RAM is not jumped at, and not used in any other way.

As an indication that the microcode has been successfully loaded, the ISTATUS[1] return byte will return a “no error” status.

5.8.3 Reading Data from the ADP

Any data from the ADP to the host is read from the ADP Status Register. The transfer is done using the ADP command format as explained in Section 12. “Annex A: ADP Commands”. Typically, each ADP command returns a status for which the host can check. The protocol is shown in Table 48 .

1. See Section 12. “Annex A: ADP Commands” for an explanation on loading ADP commands to the **ZR36710**.

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TABLE 48. Protocol of Reading Data from the ADP

Protocol
Step 1: Host writes appropriate ADP command to the ADP Data Register.
Step 2: Host writes an **NOP** ADP command to the ADP Data Register.
Step 3: Host reads the **STATUS0**[a] register, checking for **ADPRDY** = 1.
Step 4: If **ADPRDY** = 1, data is ready for the host to read from the ADP Status Register.

a. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

5.9 Reading the System Clock Counter - Reg. 0x9 (Read)

The 32 bits of the system clock counter **SCLK** (90 KHz) can be read from the System Clock Register.

TABLE 49. ZR36710 System Clock Register

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

The first 16-bit read operation from this address results in the 16 m.s. bits of **SCLK**. The second 16-bit read operation results in the 16 l.s. bits. The first read locks the value of this register until the entire read is complete (2 word reads or 4 byte reads).

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5.10 Reading the NAV Buffer in SDRAM - Reg. 0xA

Navigation packets (NV_PCK as defined in the DVD Specifications 1.0) is extracted by the **ZR36710** and stored in an allocated buffer in the SDRAM for host retrieval. The host retrieves this data via the NAV Address and Data Registers.

TABLE 50. ZR36710 NAV Address and Data Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

5.10.1 Structure of NAV Buffer in SDRAM

The NV_PCK contains information such as timing information, angle information, Highlight information, etc., that may be needed by the host for proper control of DVD players and applications.

As detailed in the DVD Specifications 1.0 document, each NV_PCK contains a 979-byte packet of PCI (Program Control Information) including the HLI (sub-picture HighLight Information) block, and a 1017-byte packet of DSI (Data Search Information). As the **ZR36710** encounters and parses a NV_PCK, both the PCI information and DSI information is zero-padded at the end of each packet to 1024 bytes each before being stored in the SDRAM. This is done to conveniently align the NV_PCK on 1K boundaries.

The NAV buffer in SDRAM has room for 8 NV_PCKs, i.e., 2 x 8 packets of 1024 bytes each. The purpose is to always store the eight most recent NV_PCKs from the bitstream. The boundaries between packs are at 1024, 2048, 3072, 4096, 5120, 6144, and 7168 words.

TABLE 51. ZR36710 NAV Buffer Allocation

NAV Buffer Start Addresses (16-bit words)	NAV Buffer Organization in SDRAM
NAV Segment 0	
0x0000	PCI data (1024 bytes)
0x0200	DSI data (1024 bytes)
NAV Segment 1	
0x0400	PCI data (1024 bytes)
0x0600	DSI data (1024 bytes)
NAV Segment 2	
0x0800	PCI data (1024 bytes)
0x0A00	DSI data (1024 bytes)
NAV Segment 3	
0x0C00	PCI data (1024 bytes)
0x0E00	DSI data (1024 bytes)
NAV Segment 4	
0x1000	PCI data (1024 bytes)
0x1200	DSI data (1024 bytes)
NAV Segment 5	
0x1400	PCI data (1024 bytes)
0x1600	DSI data (1024 bytes)
NAV Segment 6	
0x1800	PCI data (1024 bytes)
0x1A00	DSI data (1024 bytes)
NAV Segment 7	
0x1C00	PCI data (1024 bytes)
0x1E00	DSI data (1024 bytes)

5.10.2 Knowing which NAV Segment to Read

Three bits in the **STATUS1** register indicate which of the 8 segments contains the most recent NV_PCK data copied by the DVP to the NAV buffer. These bits, from m.s. to l.s., are **DVP_SW[0]** and the two **NAVBUF** bits. After a **start** host command, these bits are reset to 111b. After the first segment is written into the NAV buffer, this counter wraps around to 000b. This counter is incremented on each segment written into the NAV buffer. The counter wraps around each time it reaches 111b.

5.10.3 Host Retrieval of NV_PCKs

There are two different procedures to read the NV_PCKs, selected with bit 0 in *DVPGen2*. The big difference between each procedure is how the **ZR36710** behaves if the host does not read the NAV segments once they are filled as indicated in the notes at the bottom of the following two tables.

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TABLE 52. Protocol of Reading Data from the NAV Buffer with *DVPGen2* Bit 0 = 0

Protocol
Step 1: The **ZR36710** sets the **NAVREADY** bit in the ISR[a] to 1 once one of the eight NAV buffer segments has been filled with a complete NV_PCK. If the IMR enables this event to trigger an interrupt, then the host receives an interrupt.
Step 2: The host reads the **STATUS1**[b] register to check the **DVP_SW[0]** and **NAVBUF** bits. These bits indicate which segment number (0 to 7 as shown in Table 51) of the NAV buffer was just filled with data.
Step 3: Depending on the value of the **DVP_SW[0]** and **NAVBUF** bits, the host writes to the NAV Address Register the base address within the NAV buffer of the NV_PCK to be read. Table 51 shows the address map of the NAV buffer. Upon writing an address to this register, the **DRAMBF** bit in the **STATUS0** register is cleared. The **ZR36710** begins to queue NV_PCK data into a 32-word FIFO. This FIFO is cleared whenever an address is loaded into the NAV Address Register.
Step 4: The host checks the **STATUS0**[b] register for **DRAMBF** = 1, indicating that the device has filled the FIFO for the host to read.
Step 5: If **DRAMBF** = 1, the host reads 32 words from the NAV Data Register. After reading the last word, the **DRAMBF** bit is automatically reset to 0 and the **ZR36710** queues the next 32 words into the FIFO. As long as 32 words are read from the NAV Data Register, the host does not need to enter a new address to the NAV Address Register. The address is incremented automatically within the device.
Step 6: Steps 4 and 5 can be repeated until the entire 2048 bytes of the NV_PCK (or portion thereof) are read. The host must check that **DRAMBF** = 1 before attempting to read each group of 32 words from the NAV Data Register.
Note 1: The host may only read a portion of the NV_PCK by writing the appropriate address to the NAV Address Register (e.g. the address associated with the beginning of the HLI data within the PCI data) and reading the desired amount of bytes.
Note 2: With *DVPGen2* bit 0 = 0, if the host does not read the NAV segments and all eight segments have been filled with data, the next NV_PCK will overwrite the first NAV segment.

a. See Section 5.2 “Interrupt Status and Mask Registers, Reg. 0x2” for an explanation on reading ISR bits.

b. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

TABLE 53. Protocol of Reading Data from the NAV Buffer with *DVPGen2* Bit 0 = 1

Protocol
Step 1: The **ZR36710** sets the **NAVREADY** bit in the ISR to 1 once one of the eight NAV buffer segments has been filled with a complete NV_PCK. If the IMR enables this event to trigger an interrupt, then the host receives an interrupt.
Step 2: The host reads the **STATUS1** register to check the **DVP_SW[0]** and **NAVBUF** bits. These bits indicate which segment number (0 to 7 as shown in Table 51) of the NAV buffer was just filled with data.
Step 3: Depending on the value of the **DVP_SW[0]** and **NAVBUF** bits, the host writes to the NAV Address Register the base address within the NAV buffer of the NV_PCK to be read. Table 51 shows the address map of the NAV buffer. Upon writing an address to this register, the **DRAMBF** bit in the **STATUS0** register is cleared. The **ZR36710** begins to queue NV_PCK data into a 32-word FIFO. This FIFO is cleared whenever an address is loaded into the NAV Address Register.
Step 4: The host checks the **STATUS0** register for **DRAMBF** = 1, indicating that the device has filled the FIFO for the host to read.
Step 5: If **DRAMBF** = 1, the host reads 32 words from the NAV Data Register. After reading the last word, the **DRAMBF** bit is automatically reset to 0 and the **ZR36710** queues the next 32 words into the FIFO. As long as 32 words are read from the NAV Data Register, the host does not need to enter a new address to the NAV Address Register. The address is incremented automatically within the device.
Step 6: Steps 4 and 5 can be repeated until the entire 2048 bytes of the NV_PCK (or portion thereof) are read. The host must check that **DRAMBF** = 1 before attempting to read each group of 32 words from the NAV Data Register.
Step 7: Once the host no longer needs the data in the segment, the host must write 0x00 to *DecCntr*.
Note 1: The host may only read a portion of the NV_PCK as explained in Table 52 .
Note 2: With *DVPGen2* bit 0 = 1, if the host does not read the NAV segments, the **ZR36710** will accumulate up to seven NAV segments and will stop requesting bitstream upon receiving the beginning of the eigth NAV segment.

5.11 Writing OSD Data - Reg. 0xB and 0xC (Write)

The **ZR36710** allocates a buffer (the exact size is explained in the microcode release notes) in SDRAM dedicated for OSD data that is provided by the host. Access to this buffer is provided through the OSD Address and Data Registers.

TABLE 54. ZR36710 OSD Address and Data Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

The OSD buffer can be configured as either a single OSD plane or as two planes of equal size. In the case of two planes, the first half of the buffer is designated “plane 0” and the second half of the buffer is designated “plane 1”. The maximum size of each plane allowed is 128KB, thus if only one plane is allocated, the maximum OSD buffer size is 128KB and if two planes are allocated, the maximum OSD buffer size is 256KB. Refer to Section 9. “On-Screen Display” for a description of the OSD data format. The protocol for writing data to the OSD buffer is shown in Table 55 .

TABLE 55. Protocol of Writing Data to the OSD Buffer

Protocol
Step 1: The host writes a base address (each address points to a word, not a byte) to the OSD Address Register, indicating the starting address within the OSD buffer that OSD words will be written to. A write to this address register immediately sets **DRAMBE** = 1 in the **STATUS0** register.
Step 2: The host writes up to 32 words of OSD data to the OSD Data Register. These words are loaded into a 32-word FIFO. As soon as there is data in this FIFO, **DRAMBE** switches to 0.
Step 3: Once the 32nd word is written to the OSD Data Register, the **ZR36710** retrieves the data from the FIFO and copies it into the OSD buffer in SDRAM. Once all 32 words are retrieved from the FIFO, the **DRAMBE** bit is set to 1.
Step 4: The host checks for **DRAMBE**[a] = 1 if the host will transfer more data.
Step 5: Once **DRAMBE** = 1, the host may write up to 32 words to the OSD Data Register. The **ZR36710** will automatically increment the address pointer within the buffer so the host is not required to load a new address to the OSD Address Register.
Step 6: This process of checking for **DRAMBE** = 1 and writing 32 words to the OSD Data Register (steps 4 and 5) is repeated as frequently as necessary, depending on how much data must be written into the OSD buffer.
Step 7: If less than 32 words are written to the OSD Data Register, the host must write 0xFFFF to the OSD Address Register to indicate that there are less than 32 words in the FIFO and thus the **ZR36710** will read these words. Without writing 0xFFFF to the OSD Address Register, the **ZR36710** would have no indication to read the words in the FIFO.
Step 8: Once the host is finished writing data to the OSD Data Register (whether or not a complete 32 words were written to the FIFO), the host writes 0xFFFF to the OSD Address Register.

a. See Section 5.5 “Status Registers - Reg. 0x3, 0x4, 0x5 (Read)” for an explanation on reading status register bits.

If the OSD buffer is configured as one plane, then the entire OSD buffer is allocated to the single plane with a starting address of 0x0000. If the OSD buffer is configured as two planes, then the first half of the buffer is allocated as plane 0 with a starting address of 0x0000 and the second half of the buffer is allocated as plane 1 with a starting address of (OSD buffer size in bytes / 4).

5.12 Code Buffer Status Registers - Reg. 0xC, 0xD, 0xE (Read)

The **ZR36710** allocates three buffers within its SDRAM for each of these three types of coded data:

- Coded video data.
- Coded audio data.
- Coded sub-picture data.

The device parses the bitstream, separates each type of coded data, and places each type into its own buffer until the device retrieves the data for decoding. The fullness, or the number of bytes that have been written to each buffer, but not yet been decoded, for each buffer can be checked via reads from the Video, Audio and Sub-Picture Code Buffer Status Registers. See Section 6.5 “Stream Demultiplexing” for more information regarding demultiplexing of the bitstream and allocation of the stream data into these buffers.

TABLE 56. ZR36710 Sub-Picture, Video and Audio Code Buffer Status Registers

Address	Read Register(16 bits)	Write Register(16 bits)
0x0	Parameter Address Register	Parameter Address Register
0x1	Parameter Data Register	Parameter Data Register
0x2	Interrupt Status Register	Interrupt Mask Register
0x3	STATUS0 Register	Host Command Register
0x4	STATUS1 Register	Coded Bitstream Register
0x5	STATUS2 Register	Reserved
0x6	DVP Data Register	DVP Data Register
0x7	Device ID Register	Reserved
0x8	ADP Status Register	ADP Data Register
0x9	System Clock Register	Reserved
0xA	NAV Data Register	NAV Address Register
0xB	Reserved	OSD Address Register
0xC	Sub-Picture Code Buffer Status Register	OSD Data Register
0xD	Video Code Buffer Status Register	Reserved
0xE	Audio Code Buffer Status Register	Reserved
0xF	Reserved	Reserved

Interpretation of the Value Within the Code Buffer Status Registers

The fullness of each of these buffers is measured in 32-byte groups, for example:

- If a value of 7151 (0x1BEF) is read from the Video Code Buffer Status Register, then there are between (7151 x 32 = 228832) to (7151 x 32 + 31 = 228863) bytes in the video code buffer that have not been decoded.
- If a value of 127 (0x007F) is read from the Audio Code Buffer Status Register, then there are between (127 x 32 = 4064) to (127 x 32 + 31 = 4095) bytes in the audio code buffer that have not been decoded.
- If a value of 1128 (0x0468) is read from the Sub-Picture Code Buffer Status Register, then there are between (1128 x 32 = 36096) to (1128 x 32 + 31 = 36127) bytes in the sub-picture code buffer that have both not been released by the sub-picture decoder (SPU bytes can be “decoded”, but until the **ZR36710** has no further use for the decoded SPU (e.g. display), the decoded bytes are not released) nor been decoded.